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Phison Electronics Corporation

PS3002 CompactMedia Controller Specification

version 1.04

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Document Number : S-06030

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Revision History

Revision	History	Draft Date	Author
1.01	Support Industry level	29-Sep-2005	Adam
1.02	Add Regulator leakage current	01-May-2006	Mingren
1.03	Change the operation and storage temperature for commercial and industrial IC in electrical specification	04-Aug-2006	David
1.04	Add TTL parameters to DC Characters and add DMA feature to Pin Description	15-Nov-2006	Jenchieh

A. General Description

The PHISON PS3002 Compact Media micro-controller is the best choice for CompactFlash™ Card / MultiMedia Card / Secure Digital Card / SmartMedia™ Card / Memory Stick Card / Memory Stick Pro Card / xD-Picture Card Reader/Writer.

It is a multi-function chip with excellent performance and low cost. All devices designed by this controller do not need to have additional mechanical parts, but have the properties of fully anti vibration and extremely low power consumption.

By using this one chip solution, all the efforts from R/D to production will be greatly reduced and will also simplify the RMA problems.

B. Controller Features

Support Host Interfaces

- PCMCIA / IDE Interface
  (Support to PIO Mode 4 / Multi Word DMA Mode2 / Ultra DMA Mode 2)
- Fully compatible with CompactFlash specification version 2.0
- Fully compatible with PC Card Standard Release 8.0
- Fully compatible with the IDE standard interface
- Host Transfer Rate for PC Card / CompactFlash : 16.6MB/s (PIO4)
- Host Transfer Rate for IDE standard interface: 33.3MB/s (UDMA2)

Support Memory Card Interfaces

- Smart Media Card (SM)
- xD-Picture Card (xD)
- Memory Stick Card (MS)
- Memory Stick Pro Card (MS Pro)
- Secure Digital Card (SD)
- MultiMedia Card (MMC)
- Build-in NAND Flash Memory

Smart Media Card Interface

- Fully compatible with SmartMedia™ Electrical Specification Version 1.30
- Fully compatible with SmartMedia™ Physical Format Specification Version 1.30
- Fully compatible with SmartMedia™ Logical Format Specification Version 1.20
- Fully compatible with SmartMedia™ Standard Specification Millennium Version
- Support capacity 4/8/16/32/64/128MB
- Build-in standard Smart Media hardware ECC circuit
- Best performance with hardware sequencer control logic

xD-Picture Card Interface

- Fully compatible with xD-Picture Card™ Specification Version 1.00
- Support capacity 16 / 32 / 64 / 128 / 256 / 512 MB
- Build-in standard hardware ECC circuit.
- Best performance with hardware sequencer control logic

Memory Stick / Memory Stick Pro Interface

- Fully compatible with Memory Stick Standard Format Specification version 1.4
- Fully compatible with Memory Stick Pro Standard Format Specification version 1.00
- Auto Data CRC generating & checking
- Memory Stick Support capacity 16 / 32 / 64 / 128MB
- Memory Stick Pro Support capacity 256 / 512MB / 1GB / 2GB / 4GB

Secure Digital Card / MultiMedia Card Interface

- Fully compatible with MultiMedia Card System Specification 4.0
- Fully compatible with Secure Digital Specification 1.10
- MMC Support capacity 16 / 32 / 64 / 128 / 256 / 512MB / 1GB
- SD Support capacity 16 / 32 / 64 / 128 / 256 / 512MB /1GB / 2GB
- Auto Data CRC generating & checking
- Auto Command / Response CRC generating & checking
- Standard MMC / SPI / SD 4-bit mode interface support
- No any compatible issues with ALL kinds of MMC / SD cards

Build-In NAND Flash Memory Interface

- Build-in hardware ECC circuit (Hamming & Reed-Solomon).
- Support SLC (single level cell) NAND Flash Memory.
- Support Large Block (2K+64 bytes per page) NAND Flash Memory.
- Support MLC (multi level cell) NAND flash.

- **1T RISC uP8051 RAM Mode**
  - Internal RAM: 256 Bytes.
  - External RAM: 6KB (On Chip)

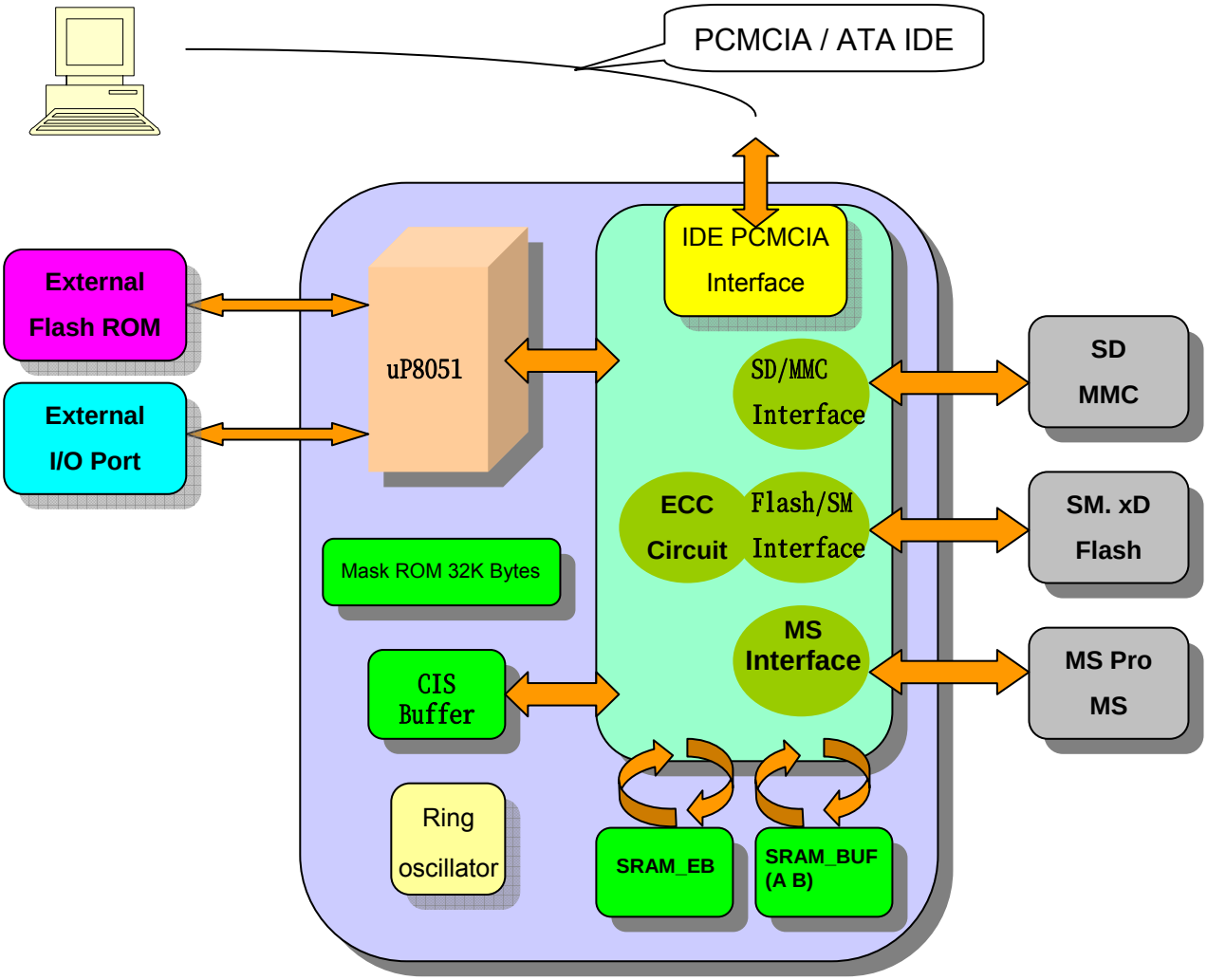
- **Support SRAM Buffer (Dual Buffer Mode):**
  - A Buffer (512 Words)
  - B Buffer (512 Words)
  - CIS Buffer (256 bytes)

- **128-Pin QFP Package**

- **Operating Voltage: 2.7V ~ 5.5V**

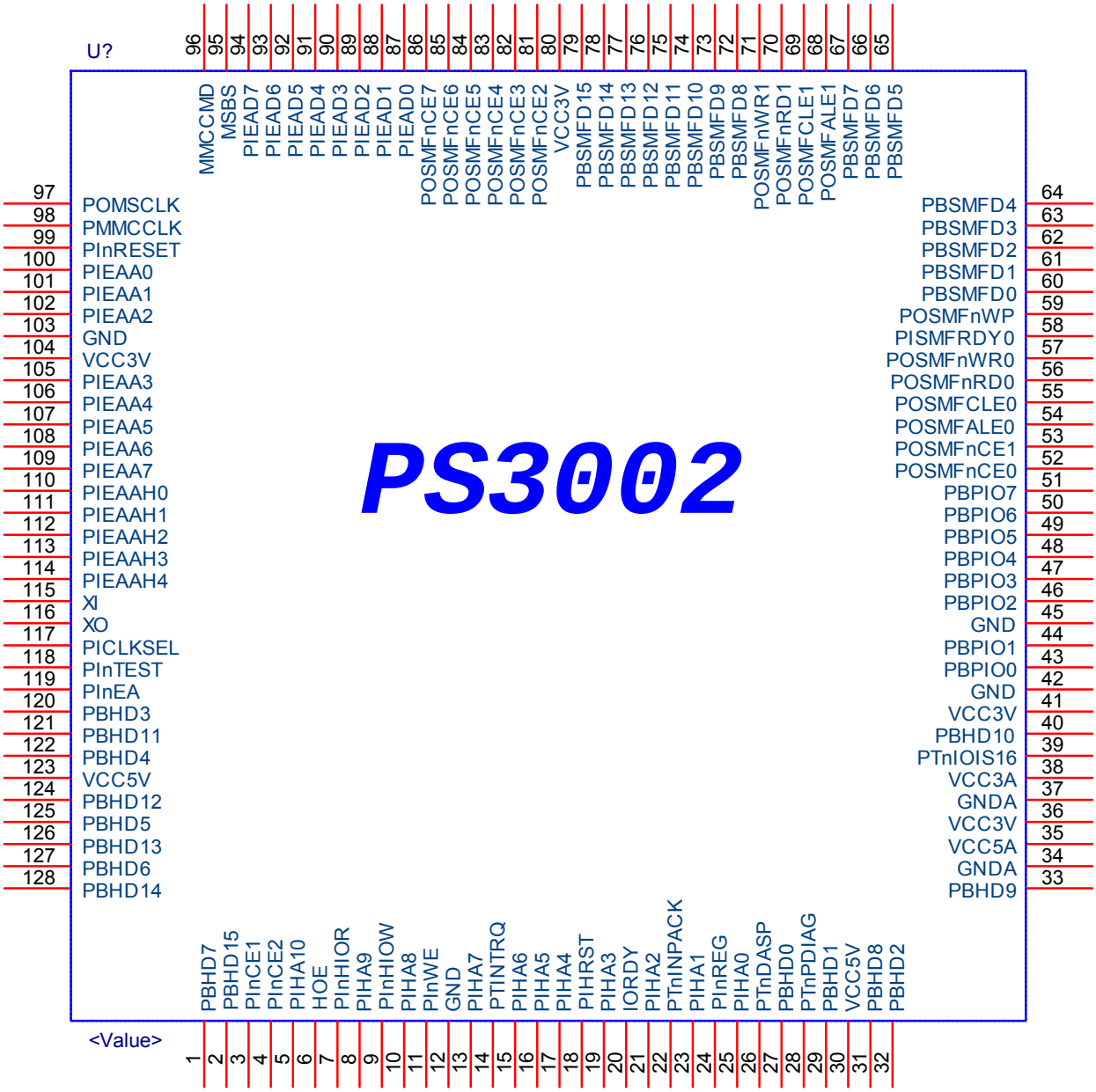
- **Power Saving implemented**

C. Block Diagram



D. Pin Assignment and Description

D1. Pin Assignment



D2. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PBHD[7]	33	PBHD[9]	65	PBSMFD[5]	97	POMSCLK
2	PBHD[15]	34	GNDA	66	PBSMFD[6]	98	PMMCCLK
3	PInCE1	35	VCC5I	67	PBSMFD[7]	99	PInRESET
4	PInCE2	36	VCC3O	68	POSMFALE1	100	PIEAA[0]
5	PIHA[10]	37	GNDA	69	POSMFCLE1	101	PIEAA[1]
6	PInHOE	38	VCC3A	70	POSMFnRD1	102	PIEAA[2]
7	PInHIOR	39	PTnIOIS16	71	POSMFnWE1	103	GND
8	PIHA[9]	40	PBHD[10]	72	PBSMFD[8]	104	VCC3I
9	PInHIOW	41	VCC3I	73	PBSMFD[9]	105	PIEAA[3]
10	PIHA[8]	42	GND	74	PBSMFD[10]	106	PIEAA[4]
11	PInHWE	43	PBPIO[0]	75	PBSMFD[11]	107	PIEAA[5]
12	GND	44	PBPIO[1]	76	PBSMFD[12]	108	PIEAA[6]
13	PIHA[7]	45	GND	77	PBSMFD[13]	109	PIEAA[7]
14	PTINTRQ	46	PBPIO[2]	78	PBSMFD[14]	110	PIEAAH[0]
15	PIHA[6]	47	PBPIO[3]	79	PBSMFD[15]	111	PIEAAH[1]
16	PIHA[5]	48	PBPIO[4]	80	VCC3I	112	PIEAAH[2]
17	PIHA[4]	49	PBPIO[5]	81	POSMFnCE[2]	113	PIEAAH[3]
18	PIHRST	50	PBPIO[6]	82	POSMFnCE[3]	114	PIEAAH[4]
19	PIHA[3]	51	PBPIO[7]	83	POSMFnCE[4]	115	XSCI
20	IORDY	52	POSMFnCE[0]	84	POSMFnCE[5]	116	XSCO
21	PIHA[2]	53	POSMFnCE[1]	85	POSMFnCE[6]	117	PICLKSEL
22	PTnINPACK	54	POSMFALE0	86	POSMFnCE[7]	118	PInTEST
23	PIHA[1]	55	POSMFCLE0	87	PIEAD[0]	119	PInEA
24	PInREG	56	POSMFnRD0	88	PIEAD[1]	120	PBHD[3]
25	PIHA[0]	57	POSMFnWE0	89	PIEAD[2]	121	PBHD[11]
26	PTnDASP	58	PISMFRDY	90	PIEAD[3]	122	PBHD[4]
27	PBHD[0]	59	POSMFnWP	91	PIEAD[4]	123	VCC5I
28	PTnPDIAG	60	PBSMFD[0]	92	PIEAD[5]	124	PBHD[12]
29	PBHD[1]	61	PBSMFD[1]	93	PIEAD[6]	125	PBHD[5]
30	VCC5I	62	PBSMFD[2]	94	PIEAD[7]	126	PBHD[13]
31	PBHD[8]	63	PBSMFD[3]	95	PBMSBS	127	PBHD[6]
32	PBHD[2]	64	PBSMFD[4]	96	PMMCCMD	128	PBHD[14]

D3. Pin Description

PCMCIA(PC Card Memory Mode/ PC Card IO Mode) / True IDE / CF Interface(41 Pins)			
No	**Pin Name**	**Dir.**	**Pin Description**
2, 128, 126, 124, 121, 40, 33, 31, 1, 127, 125, 122, 120, 32, 29, 27	PBHD[15:0]	I/O	These lines carry the Data, Commands and Status information between the host and the controller. PBHD[0] is the LSB of the Even Byte of the Word. PBHD[8] is the LSB of the Odd Byte of the Word.
			This signal is the same as the PC Card Memory Mode signal.
			In True IDE Mode all Task File operations occur in byte mode on the low order bus PBHD[0]-PBHD[7] while all data transfers are 16bit using PBHD[0]-PBHD[15].
3,4	PInCE1, PInCE2	I	These input signals are used to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on the A0 and –CE2.
			This signal is the same as the PC Card Memory Mode signal.
			In the True IDE Mode CSO is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.
5, 8, 10, 13, 15, 16, 17, 19, 21, 23, 25	PIHA[10:0]	I	These address lines along with the REG signal are used to select the following : The I/O port address registers within the CompactFlash Storage Card, the memory mapped port address registers within the CompactFlash Storage Card, a byte in the card's information structure and its configuration control and status registers.
			This signal is the same as the PC Card Memory Mode signal.
			In the True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
24	PInREG	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
			In True IDE Mode, this is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfer. While DMA operations are not active, the card shall ignore the signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.

No	Pin Name	Dir.	Pin Description
6	PInHOE	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers.
			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
			TO enable True IDE Mode this input should be grounded by the host.
11	PInHWE	I	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
			In PC Card I/O Mode, this signal is used for writing the configuration registers.
			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
7	PInHIOR	I	This signal is not used in this mode.
			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface.
			In True IDE Mode, this signal has the same function as in PC Card I/O Mode. In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in burst. In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of strobe cause data to be latched by the device.
9	PInHIOW	I	This signal is not used in this mode.
			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
			In True IDE Mode, this signal has the same function as in PC Card I/O Mode. In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.

No	Pin Name	Dir.	Pin Description
18	PIHRST	I	When the pin is high, this signal Resets the CompactFlash Storage Card. The CompactFlash Storage Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
			This signal is the same as the PC Card Memory Mode signal.
			In the True IDE Mode this input pin is the active low hardware reset from the host.
22	PTnINPACK	O	This signal is not used in this mode.
			The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU
			This signal is a DMA Request that is used for DMA data transfer between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. This signal shall not be driven when the device is not selected. If there is no hardware support for DMA mode in the host, this output signal is not used and should be connected at the host.
14	PTINTRQ	O	In Memory Mode this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Storage Card has been powered up with +RESET continuously disconnected or asserted.
			I/O Operation After the CompactFlash Storage Card has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
			In True IDE Mode signal is the active high Interrupt Request to the host.

No	Pin Name	Dir.	Pin Description
39	PTnIOIS16	O	Memory Mode – The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
			I/O Operation – When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the – I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.
28	PTnPDIAG	I/O	Memory Mode – This signal is asserted high (BVD1 is not supported).
			I/O Operation – This signal is asserted low to alert the host to changes is the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register
			In True IDE Mode – This input/ output is the Pass Diagnostic signal in the Master/ Slave handshake protocol
26	PTnDASP	I/O	Memory Mode –This signal is asserted high (BVD2 is not supported).
			I/O Operation – This signal is held negated.
			In True IDE Mode – this input/ output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
20	IORDY	O	Memory Mode – This signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress
			I/O Operation – This signal is the same as the PC Card Memory Mode signal
			In True IDE Mode – this output signal may be used as IORDY In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is ready to receive Ultra DMA data-in bursts. In True IDE Mode, when Ultra DMA mode DMA Read is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of strobe cause data to be latched by the host.

Smart Media (FLASH) Interface(50 Pins)			
No	**Pin Name**	**Dir.**	**Pin Description**
86, 85, 84, 83, 82, 81, 53, 52	POSMFnCE[7:0]	I/O	Flash Chip Enable, Low active.
109,108, 107,106, 105,104, 103,102, 94, 93, 92, 91, 90, 89, 88, 87, 79, 78, 77, 76, 75, 74, 73, 72, 67, 66, 65, 64, 63, 62, 61, 60	PBSMFD[31:0]	I/O	Flash Data Bus
54, 68	POSMFALE0, POSMFALE1	O	Flash Address Latch Enable, High active.
55, 69	POSMFCLE0, POSMFCLE1	O	Flash Command Latch Enable, High active.
56, 70	POSMFnRD0, POSMFnRD1	O	Flash Read Control signal, Low active.
57, 71	POSMFnWE0, POSMFnWE1	O	Flash Write Control signal, Low active.
59	POSMFnWP	I/O	Flash Write Protect Control signal, Low active.
58	PISMFRDY	I	Flash Ready/Busy signal.
MS & MSPRO Interface(6 Pins)			
No	**Pin Name**	**Dir.**	**Pin Description**
95	PBMSBS	I/O	MS/MSPRO Serial protocol Bus State signal.
79, 78, 77, 76	PBMSIO[3:0]	I/O	MS/MSPRO Data Line [3:0]. *Note1
97	POMSCLK	O	MS/MSPRO Serial protocol Clock signal.
MMC & SD Interface(6 Pins)			
No	**Pin Name**	**Dir.**	**Pin Description**
96	PMMCCMD	I/O	MMC/SD Command/Respond.
75, 74, 73, 72	PMMCD[3:0]	I/O	MMC/SD Data Line [3:0]. *Note1
98	PMMCCLK	O	MMC/SD Clock.

Global Signal(28 Pins)			
No	**Pin Name**	**Dir.**	**Pin Description**
99	PInRESET	I	Reset Signal
117	PICLKSEL	I	External Clock Select Signal.
118	PInTEST	I	Test Mode Signal.
119	PInEA	I	EAMODE Select Signal.
115	XSCI	I	External Crystal Clock In
116	XSCO	O	External Crystal Clock Out
51, 50, 49, 48, 47, 46, 44, 43	PBPIO[7:0]	I/O	uP Port1[7:0]
30, 35, 123	VCC5I	VCC	5V
41, 80, 104	VCC3I	VCC	3.3V
38	VCC3A	VCC	Low Voltage Detector Input
36	VCC3O	VCC	3.3V(Regulator Output)
12, 42, 45, 103	GND	GND	
34, 37	GNDA	GND	

***Note1 :** Share Pins with Flash Interface

E. System Power Consumption

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Iccr	Read current	5V	-	75	-	mA
Iccw	Write current	5V	-	75	-	mA
Ipd	Power down current	5V	-	-	0.4	mA
Iccr	Read current	3.3V	-	55	-	mA
Iccw	Write current	3.3V	-	55	-	mA
Ipd	Power down current	3.3V	-	-	0.3	mA
Ireg	Regulator leakage current	3.3V	-	-	0.12	mA

F. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit	Remark
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V	
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V	
3	Ta	Operating Temperature	0	+70	℃	Commercial version
4	Tst	Storage Temperature	0	+85	℃	Commercial version
5	Ta	Operating Temperature	-40	+85	℃	Industry version
6	Tst	Storage Temperature	-40	+100	℃	Industry version

Parameter	Symbol	Min	Typ	MAX	Unit
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

G. DC Characters

DC characteristics of 5.0V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Vil	Input Low Voltage	CMOS	-	-	0.3 x Vcc	V
Vih	Input High Voltage		0.7 x Vcc	-	-	V
Vil	Input Low Voltage	TTL	-	-	0.8	V
Vih	Input High Voltage		2.0	-	-	V
Vol	Output Low voltage	|Iol| = 8 ~ 12 mA	-	-	0.4	V
Voh	Output High voltage	|Ioh| = 8 ~ 12 mA	3.5	-	-	V
Rpu	Input Pull-Up Resistance	Vin = 0	30	50	125	KΩ
Rpd	Input Pull-Down Resistance	Vin = VCC5I	30	50	125	KΩ
Iin	Input Leakage Current	No pull-up or pull down	-10	±1	10	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

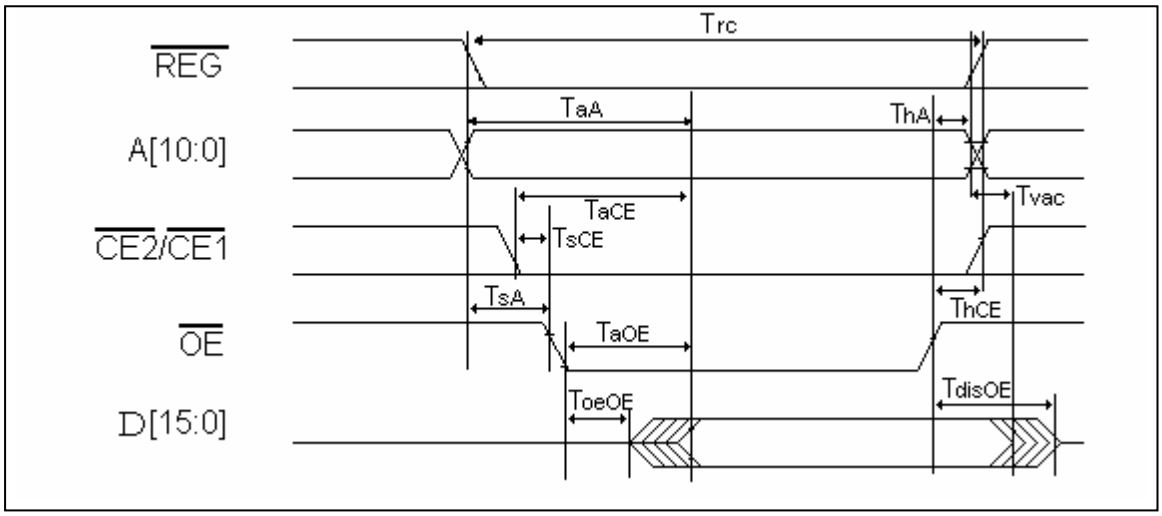
DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Vil	Input Low Voltage	CMOS	-	-	0.3 x Vcc	V
Vih	Input High Voltage		0.7 x Vcc	-	-	V
Vil	Input Low Voltage	TTL	-	-	0.8	V
Vih	Input High Voltage		2.0	-	-	V
Vol	Output Low voltage	|Iol| = 8 ~ 12 mA	-	-	0.4	V
Voh	Output High voltage	|Ioh| = 8 ~ 12 mA	2.4	-	-	V
Rpu	Input Pull-Up Resistance	Vin = 0	40	75	190	KΩ
Rpd	Input Pull-Down Resistance	Vin = VCC3I	40	75	190	KΩ
Iin	Input Leakage Current	No pull-up or pull down	-10	±1	10	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

H. AC Characters

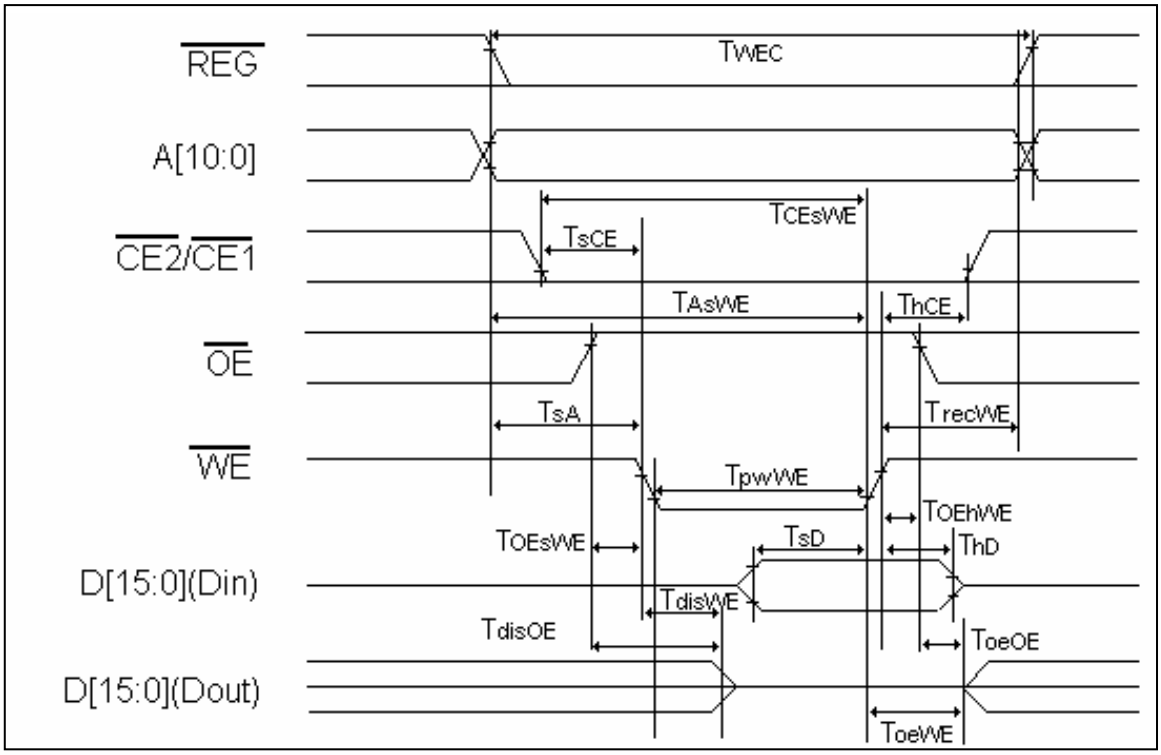
H1. PCMCIA Interface

[Attribute Memory Read Timing]



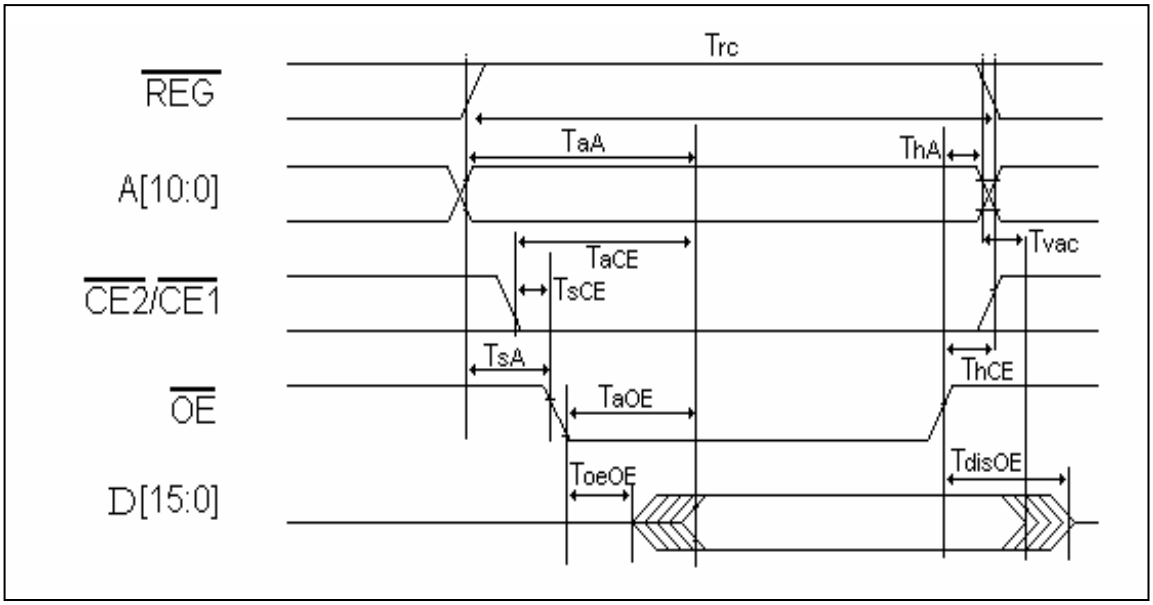
Symbol	Parameter	Min	Max	Unit
Trc	Read Cycle Time	250	-	ns
TaA	Address Access Time	-	250	ns
TaCE	Card Enable Access Time	-	250	ns
TaOE	Output Enable Access Time	-	125	ns
TdisOE	Output Disable Time from $\overline{OE}$	-	100	ns
ToeOE	Output Enable Time from $\overline{OE}$	5	-	ns
Tvac	Data Valid from Address Change	0	-	ns
TsA	Address Setup Time	30	-	ns
ThA	Address Hold Time	20	-	ns
TsCE	Card Enable Setup Time	0	-	ns

[Attribute Memory Write Timing]



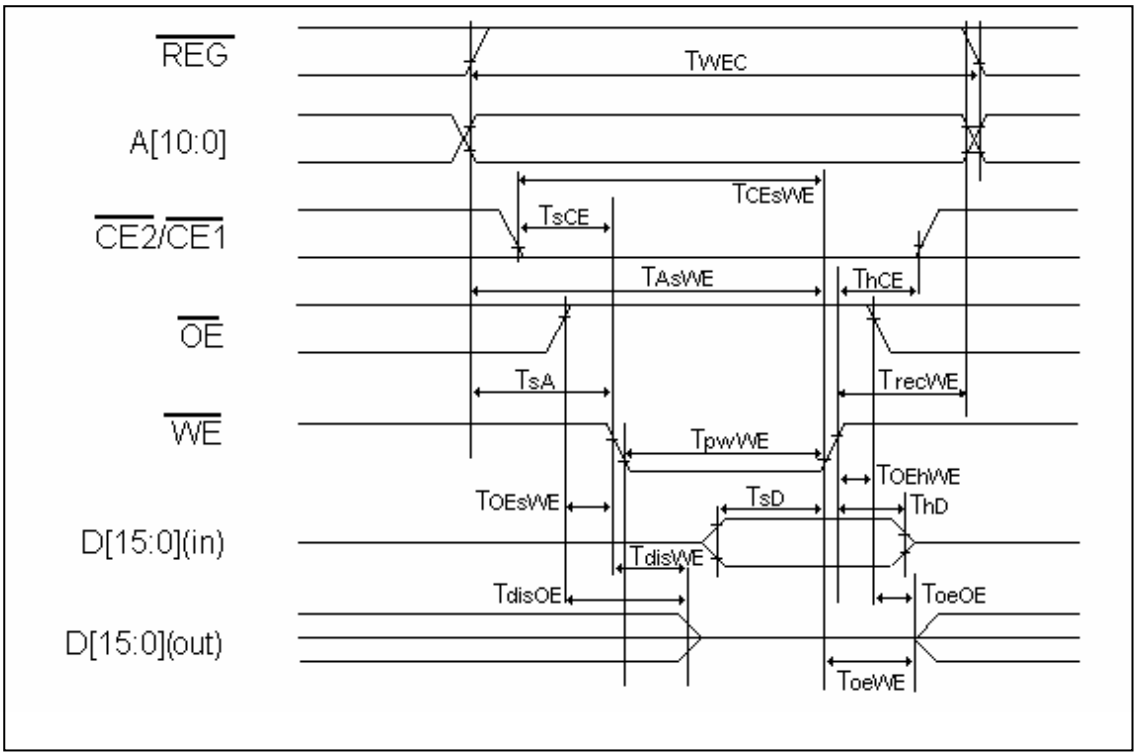
Symbol	Parameter	Min	Max	Unit
TWEC	Write Cycle Time	250	-	ns
TpwWE	Write Pulse Width	150	-	ns
TsA	Address Setup Time	30	-	ns
TasWE	Address Setup Time for $\overline{WE}$	180	-	ns
TCEsWE	Card Enable Setup Time for $\overline{WE}$	180	-	ns
TsD	Data Setup before $\overline{WE}$	30	-	ns
ThD	Data Hold Time	0	-	ns
TrecWE	Write Recover Time	0	-	ns
TdisWE	Output Disable Time from $\overline{WE}$	-	100	ns
TdisOE	Output Disable Time from $\overline{OE}$	-	100	ns
ToeWE	Output Enable Time from $\overline{WE}$	5	-	ns
ToeOE	Output Enable Time from $\overline{OE}$	5	-	ns
TOEsWE	Output Enable Setup from $\overline{WE}$	10	-	ns
TOEhWE	Output Enable Hold from $\overline{WE}$	10	-	ns
TsCE	Card Enable Setup Time	0	-	ns
ThCE	Card Enable Hold Time	0	-	ns

[Common Memory Read Timing]



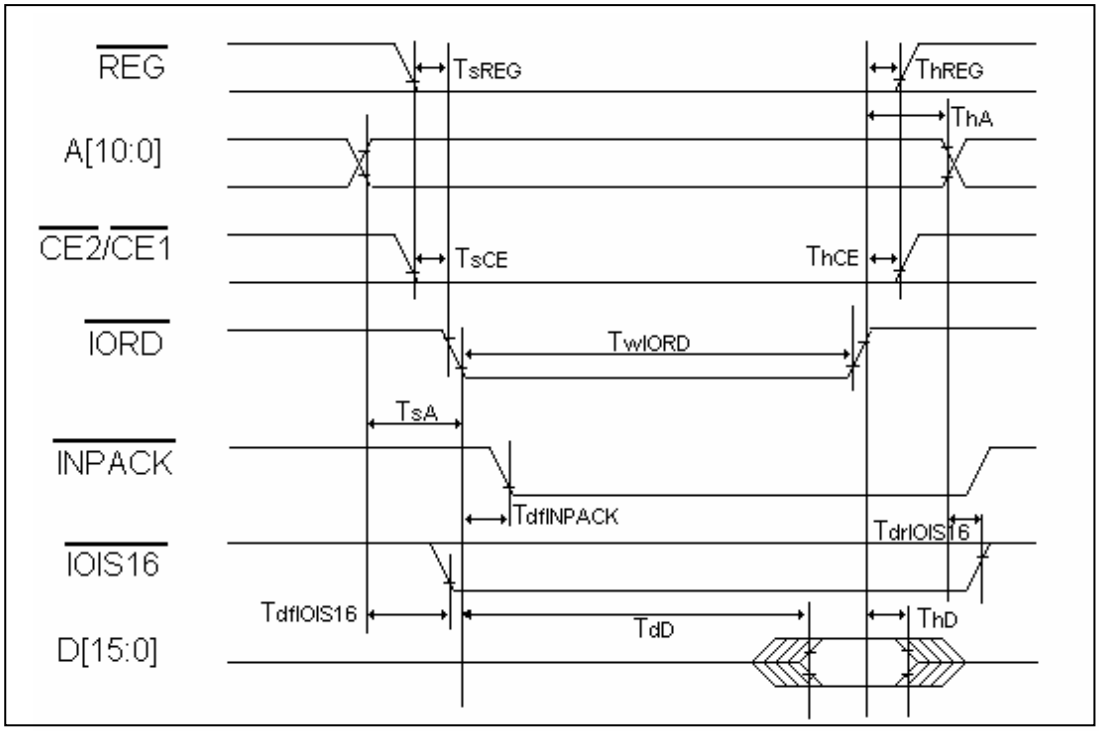
Symbol	Parameter	Min	Max	Unit
Trc	Read Cycle Time	250	-	ns
TaA	Address Access Time	-	250	ns
TaCE	Card Enable Access Time	-	250	ns
TaOE	Output Enable Access Time	-	125	ns
TdisOE	Output Disable Time from $\overline{OE}$	-	100	ns
ToeOE	Output Enable Time from $\overline{OE}$	5	-	ns
Tvac	Data Valid from Address Change	0	-	ns
TsA	Address Setup Time	30	-	ns
ThA	Address Hold Time	20	-	ns
TsCE	Card Enable Setup Time	0	-	ns
ThCE	Card Enable Hold Time	20	-	ns

[Common Memory Write Timing]



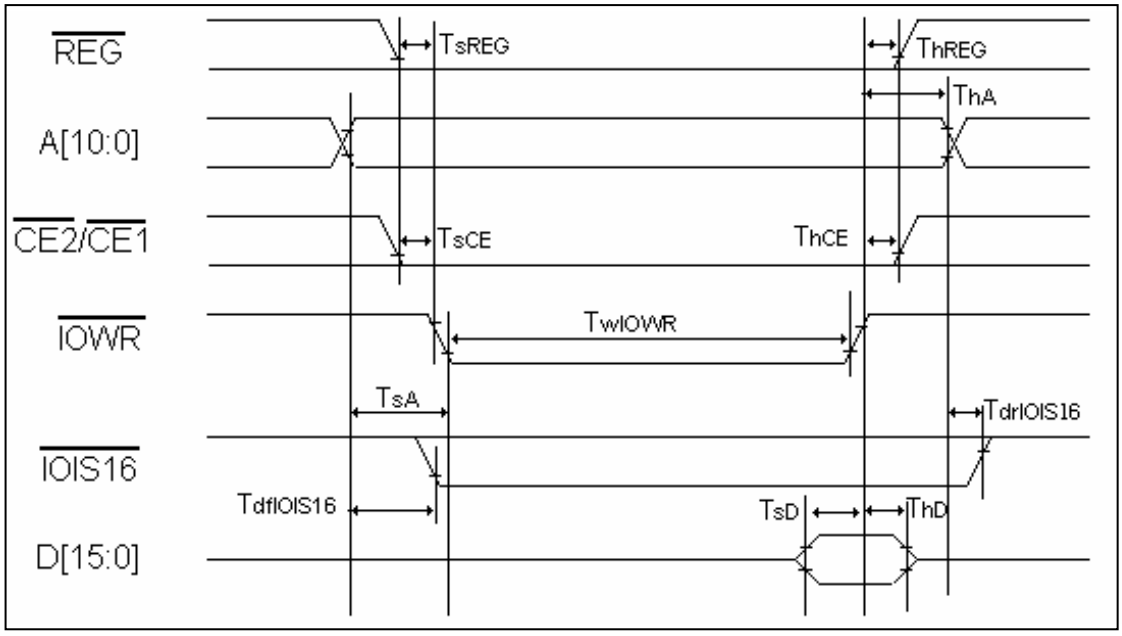
Symbol	Parameter	Min	Max	Unit
TWEC	Write Cycle Time	250	-	ns
TpwWE	Write Pulse Width	150	-	ns
TsA	Address Setup Time	30	-	ns
TAsWE	Address Setup Time for $\overline{WE}$	180	-	ns
TCEsWE	Card Enable Setup Time for $\overline{WE}$	180	-	ns
TsD	Data Setup before $\overline{WE}$	30	-	ns
ThD	Data Hold Time following $\overline{WE}$	0	-	ns
TrecWE	Write Recover Time	0	-	ns
TdisWE	Output Disable Time from $\overline{WE}$	-	100	ns
TdisOE	Output Disable Time from $\overline{OE}$	-	100	ns
ToeWE	Output Enable Time from $\overline{WE}$	5	-	ns
ToeOE	Output Enable Time from $\overline{OE}$	5	-	ns
TOEsWE	Output Enable Setup from $\overline{WE}$	10	-	ns
TOEhWE	Output Enable Hold from $\overline{WE}$	10	-	ns
TsCE	Card Enable Setup Time	0	-	ns
ThCE	Card Enable Hold Time	0	-	ns

[I/O Read Timing]



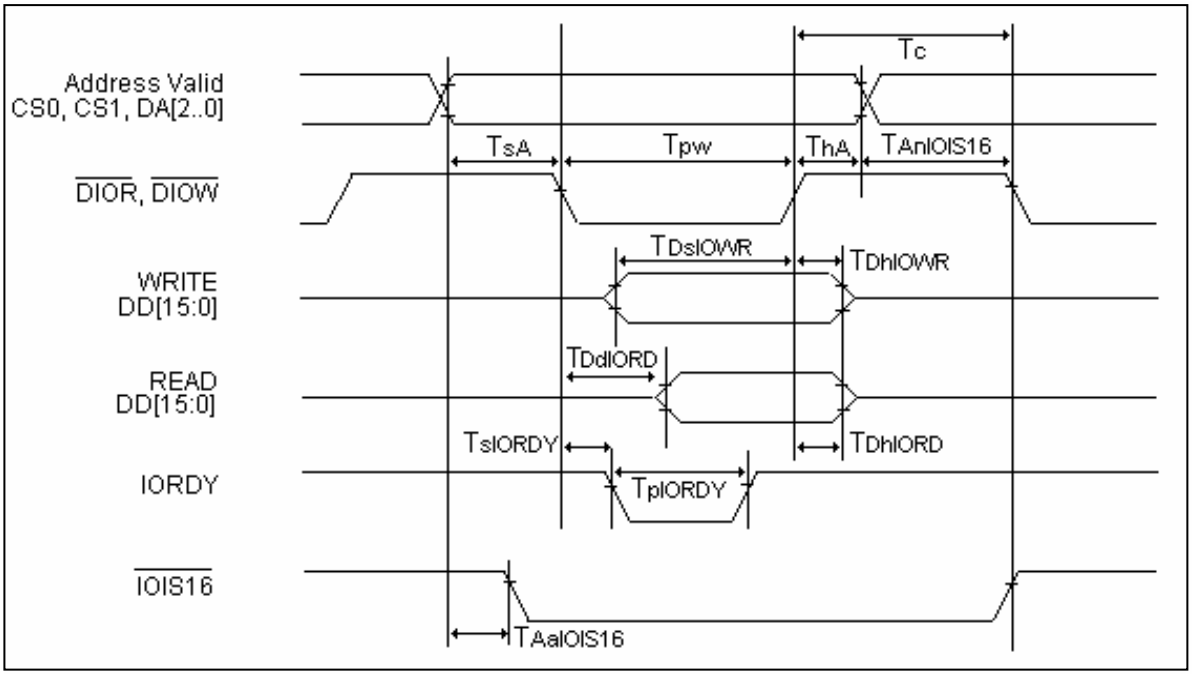
Symbol	Parameter	Min	Max	Unit
TdD	Data Delay after $\overline{IORD}$	-	100	ns
ThD	Data Hold following $\overline{IORD}$	0	-	ns
TwIORD	$\overline{IORD}$ Width Time	165	-	ns
TsA	Address Setup before $\overline{IORD}$	70	-	ns
ThA	Address Hold following $\overline{IORD}$	20	-	ns
TsCE	$\overline{CE}$ Setup Before $\overline{IORD}$	5	-	ns
ThCE	$\overline{CE}$ Hold following $\overline{IORD}$	20	-	ns
TsREG	$\overline{REG}$ Setup Before $\overline{IORD}$	5	-	ns
ThREG	$\overline{REG}$ Hold following $\overline{IORD}$	0	-	ns
TdfINPACK	$\overline{INPACK}$ Delay Falling from $\overline{IORD}$	0	45	ns
TdrINPACK	$\overline{INPACK}$ Delay Rising from $\overline{IORD}$	0	45	ns
TdfIOIS16	$\overline{IOIS16}$ Delay Falling from Address	-	35	ns
TdrIOIS16	$\overline{IOIS16}$ Delay Rising from Address	-	35	ns

[I/O Write Timing]



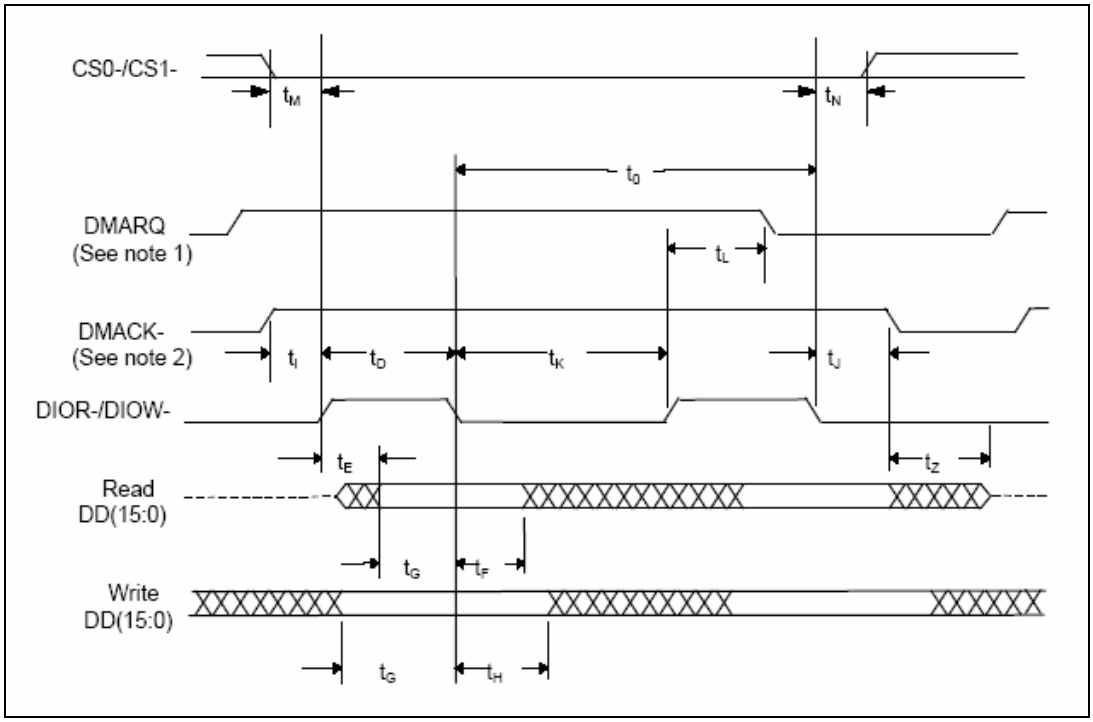
Symbol	Parameter	Min	Max	Unit
TsD	Data Setup before $\overline{IOWR}$	30	-	ns
ThD	Data Hold following $\overline{IOWR}$	30	-	ns
TwIOWR	$\overline{IOWR}$ Width Time	165	-	ns
TsA	Address Setup before $\overline{IOWR}$	70	-	ns
ThA	Address Hold following $\overline{IOWR}$	20	-	ns
TsCE	$\overline{CE}$ Setup Before $\overline{IOWR}$	5	-	ns
ThCE	$\overline{CE}$ Hold following $\overline{IOWR}$	20	-	ns
TsREG	$\overline{REG}$ Setup Before $\overline{IOWR}$	5	-	ns
ThREG	$\overline{REG}$ Hold following $\overline{IOWR}$	0	-	ns
TdfIOIS16	$\overline{IOIS16}$ Delay Falling from Address	-	35	ns
TdrIOIS16	$\overline{IOIS16}$ Delay Rising from Address	-	35	ns

H2. IDE Interface Timing (PIO Mode 4)



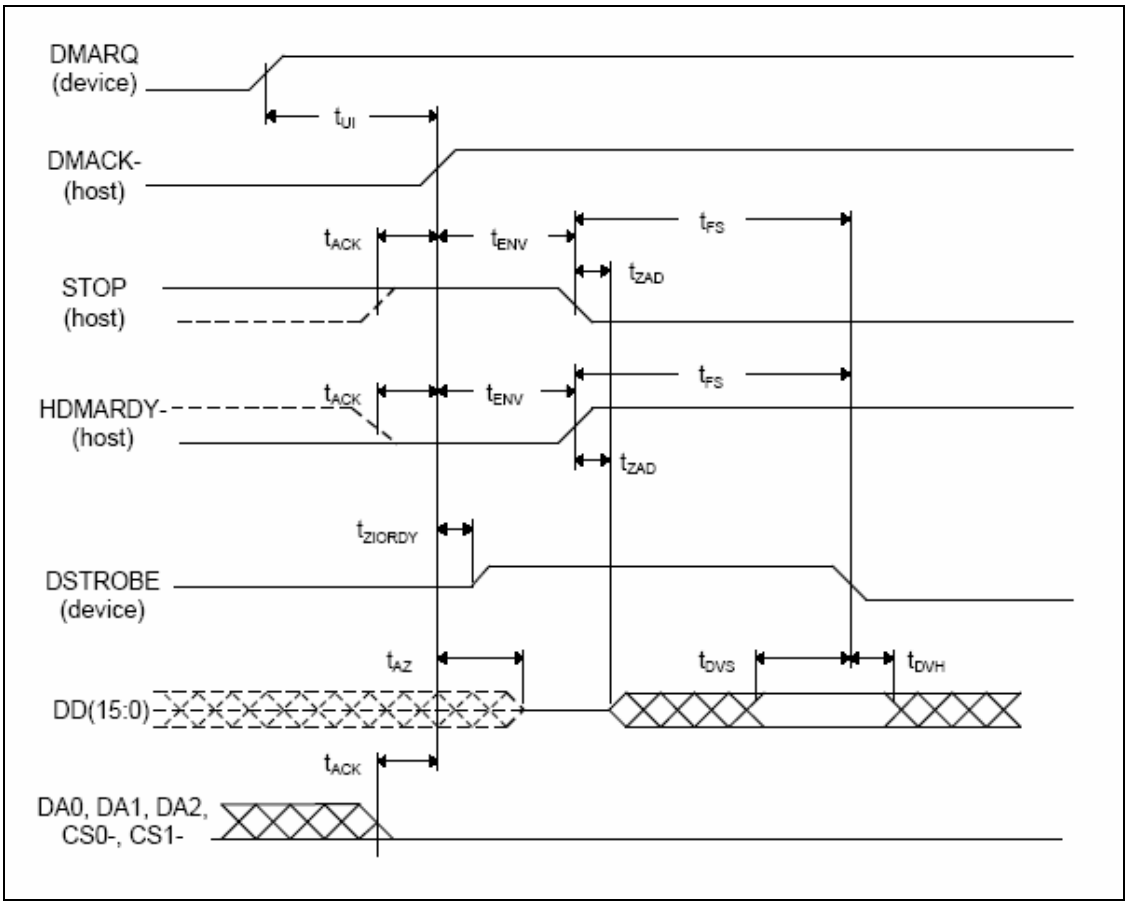
Symbol	Parameter	Min	Max	Unit
Tc	Cycle Time	120	-	ns
TsA	Address Setup before $\overline{IORD}$, $\overline{IOWR}$	25	-	ns
ThA	Address Hold following $\overline{IORD}$, $\overline{IOWR}$	10	-	ns
Tpw	$\overline{IORD}$, $\overline{IOWR}$ Pulse Width	60	-	ns
TDsIOWR	Data Setup before $\overline{IOWR}$	20	-	ns
TDhIOWR	Data Hold Following $\overline{IOWR}$	10	-	ns
TDdIORD	Data Delay After $\overline{IORD}$	-	20	ns
TDhIORD	Data Hold Following $\overline{IORD}$	5	-	ns
TAaIOIS16	$\overline{IOIS16}$ Delay Falling from Address	-	15	ns
TAnIOIS16	$\overline{IOIS16}$ Delay Rising from Address	-	15	ns
TsIORDY	IORDY Setup Time	-	35	ns
ThIORDY	IORDY Pulse Time	-	1250	ns

H3. Multi Word DMA2



Symbol	Parameter	Min	Max	Unit
t_0	Cycle Time	120	-	ns
t_D	DIOR-/DIOW-	70	-	ns
t_E	DIOR- data access	-	50	ns
t_F	DIOR- data hold	5	-	ns
t_G	DIOR-/DIOW- data setup	20	-	ns
t_H	DIOW- data hold	10	-	ns
t_I	DMACK to DIOR-/DIOW- setup	0	-	ns
t_J	DIOR-/DIOW- to DMACK hold	5	-	ns
t_{KR}	DIOR- negated pulse width	25	-	ns
t_{KW}	DIOW- negated pulse width	25	-	ns
t_{LR}	DIOR- to DMARQ delay	-	35	ns
t_{LW}	DIOW- to DMARQ delay	-	35	ns
t_M	CS(1:0) valid to DIOR-/DIOW-	25	-	ns
t_N	CS(1:0) hold	10	-	ns
t_Z	DMACK- to tristate	-	25	ns

H4. Ultra DMA2

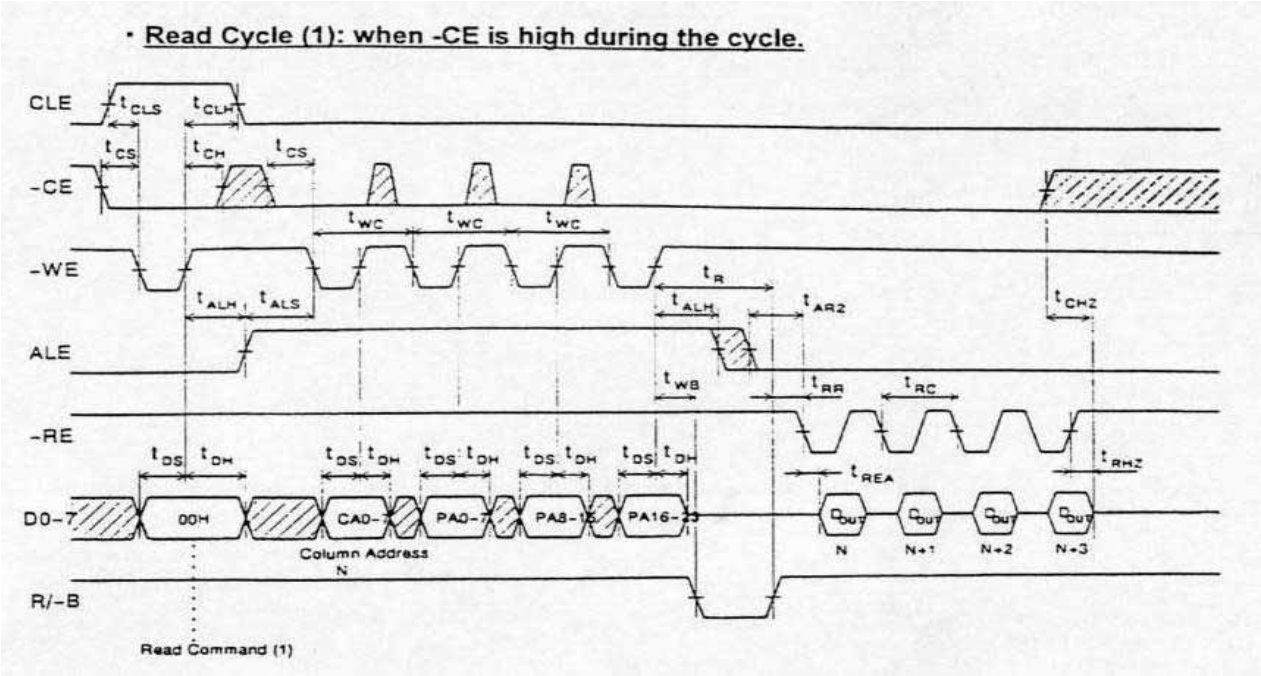


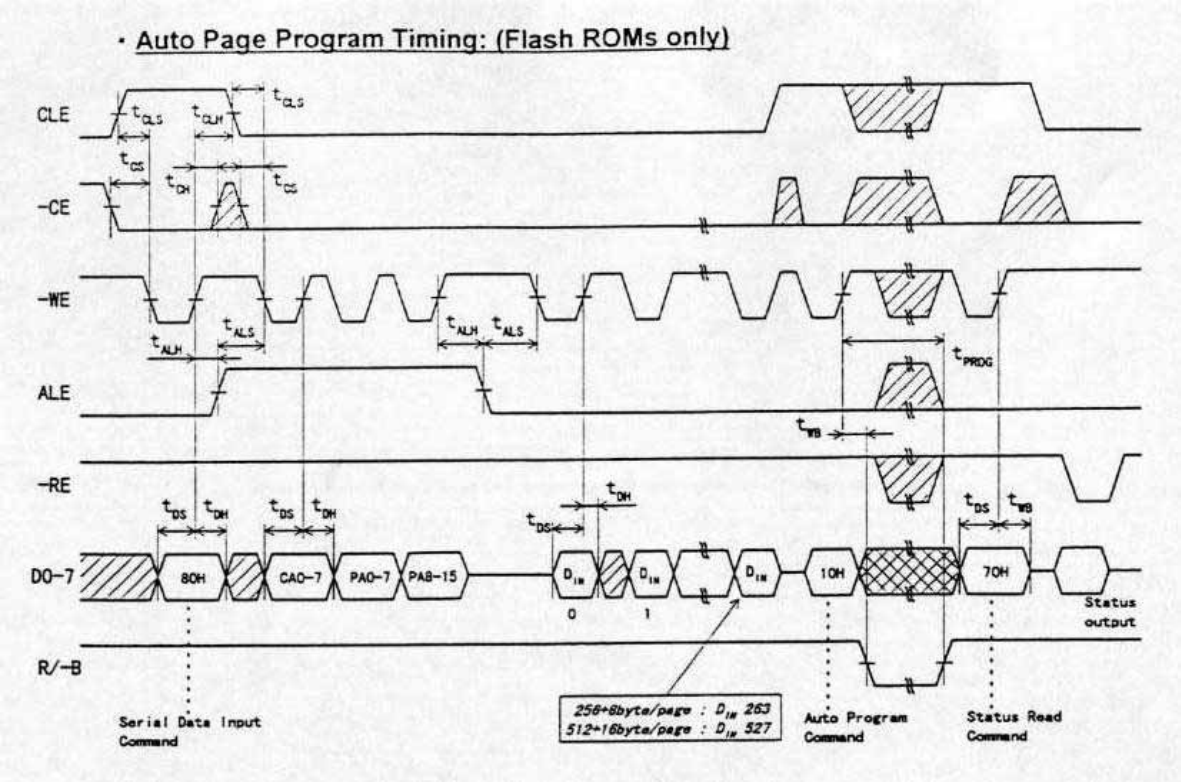
Symbol	Comment	Min	Max	Unit
t_{2CYC}	Typical sustained average two cycle time	120	-	ns
t_{CYC}	Cycle time allowing for assymetry and clock variations (from STROBE edge to STROBE edge)	55	-	ns
t_{2CYC}	Two cycle time allowing for clock variations(from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	117	-	ns
t_{DS}	Data setup time (at recipient)	7	-	ns
t_{DH}	Data hold time (at recipient)	5	-	ns
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	34	-	ns

Symbol	Comment	Min	Max	Unit
t_{DVH}	Data valid hold time at sender (from data bus being valid until STROBE edge)	6	-	ns
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	0	170	ns
t_{LI}	Limited interlock time	0	150	ns
t_{MLI}	Interlock time with minimum	20	-	ns
t_{UI}	Unlimited interlock time	0	-	ns
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	ns
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	ns
t_{ZAD}		0	-	ns
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	ns
t_{SR}	STROBE to DMARDY time (if DMARDY- is negated before this long after STROBE edge, the recipient shall receive no more than one additional data word)	-	20	ns
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	50	ns
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	100	-	ns
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	ns
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	ns
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	ns
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50	-	ns

H5. Card Interface Timing

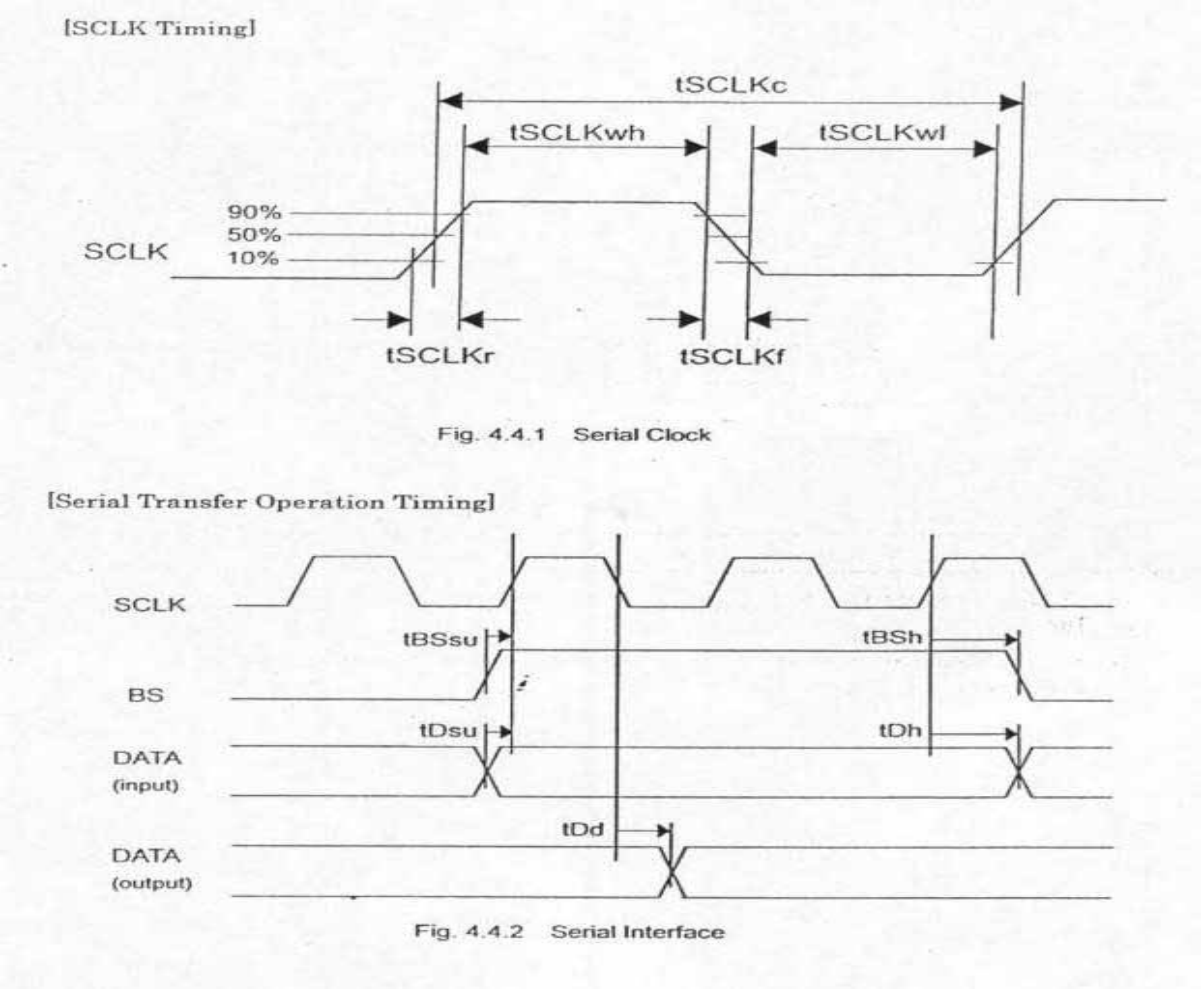
H5.1 Smart Media Interface Timing





Symbol	Parameter	Typ.	Unit
t_{CLS}	CLE Set up Time	85	ns
t_{CLH}	CLE Hold Time	85	ns
t_{CS}	-CE Set up Time	14.5	us
t_{CH}	-CE Hold Time	120	us
t_{WP}	-WE Pulse Width		ns
t_{ALS}	ALE Set up Time	165	ns
t_{ALH}	ALE Hold Time	80	ns
t_{DS}	Data Set up Time	80	ns
t_{DH}	Data Hold Time	80	ns
t_{WC}	Write Cycle Time	240	ns
t_{WH}	-WE High Hold Time	165	ns
t_{RR}	Ready to –RE Low	3.5	Us
t_{RC}	Read Cycle Time	160	ns
t_{REA}	-RE Access Time (Serial Data Access)	12.5	ns
t_{CEH}	-CE High Hold Time (at the Last Serial Read)	10	us
t_{REAID}	-RE Access Time (ID Read)	26	ns
t_{RHZ}	-RE High to Output Hi-Z	8.3	ns
t_{CHZ}	-CE High to Output Hi-Z	85	ns
t_{REH}	-RE High Hold Time	20	ns
t_{IR}	Output Hi-Z to –RE Low	480	ns
t_{RSTO}	-RE Access Time (Status Read)	15	ns
t_{WHR}	-WE High to –RE Low	9.5	us
t_{AR1}	ALE Low to –RE Low (address register read, ID read)	9.5	us
t_{CR}	-CE Low to –RE Low (data register read, ID read)	10.2	us
t_{WB}	-WE High to Busy	33	ns
t_{AR2}	ALE Low to –RE Low (read cycle)	9.45	us
t_{RB}	Last –RE High to Busy (at Sequential read)	65	ns

H5.2 Memory Stick Interface Timing



Signal	Parameter	Symbol	Typ.	Unit
SCLK	Cycle	tSCLKc	80	nsec
	H pulse length	tSCLKwh	25	nsec
	L pulse length	tSCLKwl	35	nsec
	Rise time	tSCLKr	10	nsec
	Fall time	tSCLKf	10	nsec
BS	Set-up time	tBSsu	38	nsec
	Hold time	tBSh	118	nsec
DATA	Set-up time	tDsu	35	nsec
	Hold time	tDh	43	nsec
	Output delay time	tDd	8	nsec

H5.3 Memory Stick PRO Interface Timing

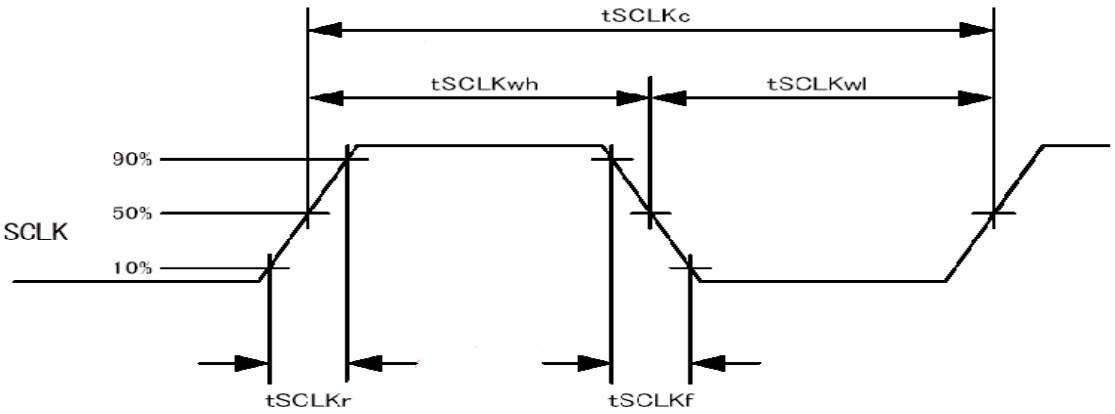


Fig. 4.4.1. Serial Clock

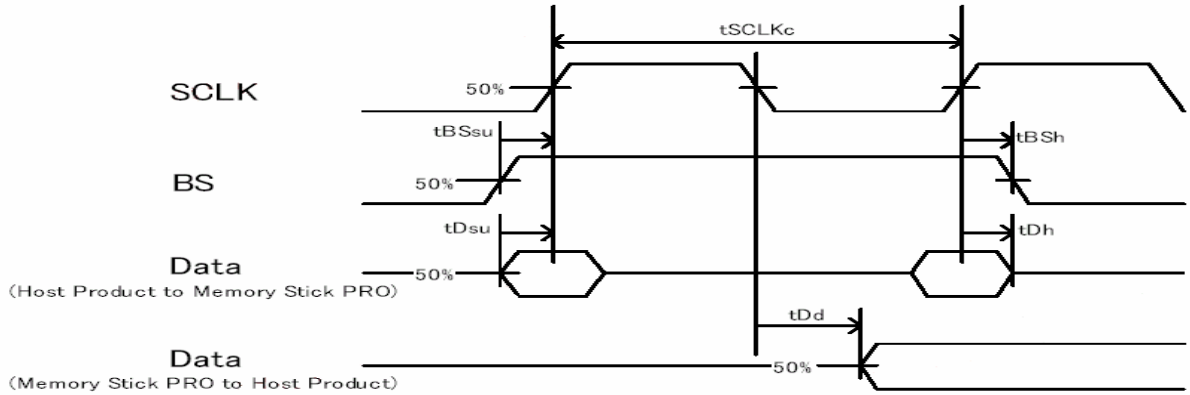
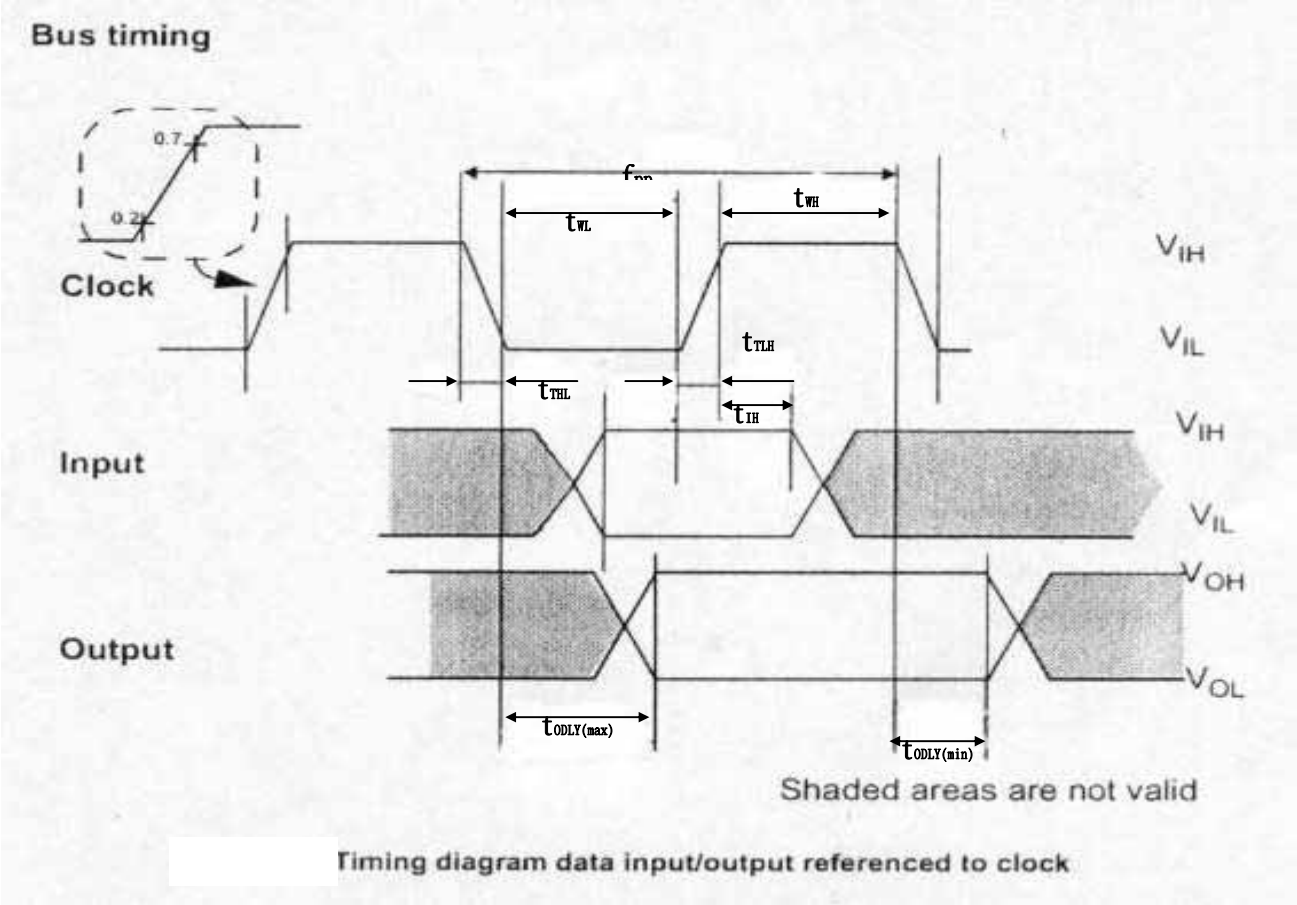


Fig. 4.4.2. Serial Transfer Operation Timing

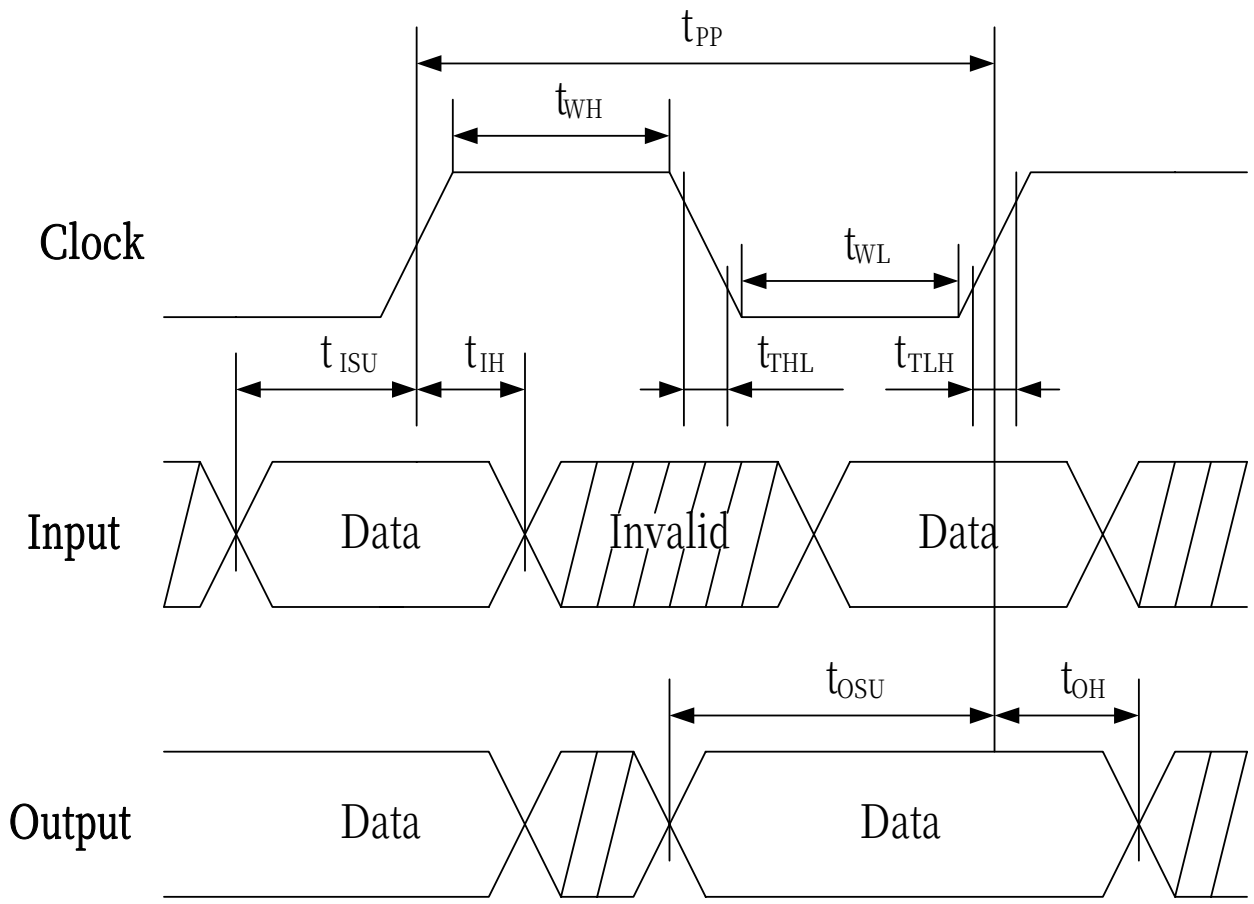
Signal	Parameter	Symbol	Typ.	Unit
SCLK	Cycle	tSCLKc	80	nsec
	H pulse length	tSCLKwh	25	nsec
	L pulse length	tSCLKwl	35	nsec
	Rise time	tSCLKr	10	nsec
	Fall time	tSCLKf	10	nsec
BS	Set-up time	tBSsu	38	nsec
	Hold time	tBSh	118	nsec
DATA	Set-up time	tDsu	35	nsec
	Hold time	tDh	43	nsec
	Output delay time	tDd	8	nsec

H5.4 SD Interface Timing



Parameter	Symbol	Typ	Unit
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}) T=25℃			
Clock frequency Data Transfer Mode	f_{pp}	12.5	MHz
Clock frequency Identification Mode (the low freq. is required for MultiMediaCard compatibility)	f_{OD}	400	KHz
Clock low time	t_{WL}	32	ns
Clock high time	t_{WH}	32	ns
Clock rise time	t_{TLH}	9	ns
Clock fall time	t_{THL}	7	ns
Input set-up time	t_{ISU}	36	ns
Input hold time	t_{IH}	42	ns
Output Delay time	t_{ODLY}	5	ns

H5.5 MMC Interface Timing



Data must always be sampled on the rising edge of the clock.

High Speed Card Interface Timing:

Parameter	Symbol	Min	Max	Unit
Clock CLK				
Clock frequency Data Transfer Mode(PP)	f_{PP}	0	26/52	MHz
Clock frequency Identification Mode(OD)	f_{OD}	0	400	kHz
Clock low time	t_{WL}	6.5	-	ns
Clock rise time	t_{TLH}	-	3	ns
Clock fall time	t_{THL}	-	3	ns
Inputs CMD, DAT (referenced to CLK)				
Input set-up time	t_{ISU}	3	-	ns
Input hold time	t_{IH}	3	-	ns
Outputs CMD, DAT (referenced to CLK)				
Output set-up time	t_{OSU}	5	-	ns
Output hold time	t_{OH}	5	-	ns
Signal rise time	t_{rise}	-	3	ns
Signal fall time	t_{fall}	-	3	ns

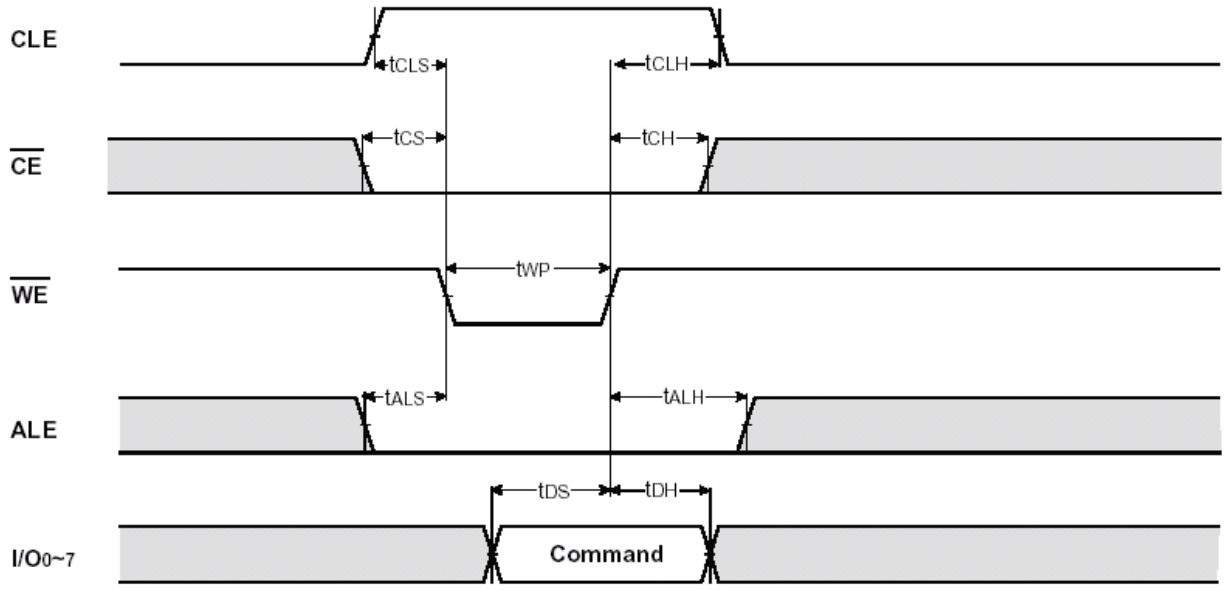
Backwards Compatible Card Interface Timing:

Parameter	Symbol	Min	Max	Unit
Clock CLK				
Clock frequency Data Transfer Mode(PP)	f_{PP}	0	20	MHz
Clock frequency Identification Mode(OD)	f_{OD}	0	400	kHz
Clock low time	t_{WL}	10	-	ns
Clock rise time	t_{TLH}	-	10	ns
Clock fall time	t_{THL}	-	10	ns
Inputs CMD, DAT (referenced to CLK)				
Input set-up time	t_{ISU}	3	-	ns
Input hold time	t_{IH}	3	-	ns
Outputs CMD, DAT (referenced to CLK)				
Output set-up time	t_{OSU}	13.1	-	ns
Output hold time	t_{OH}	9.7	-	ns

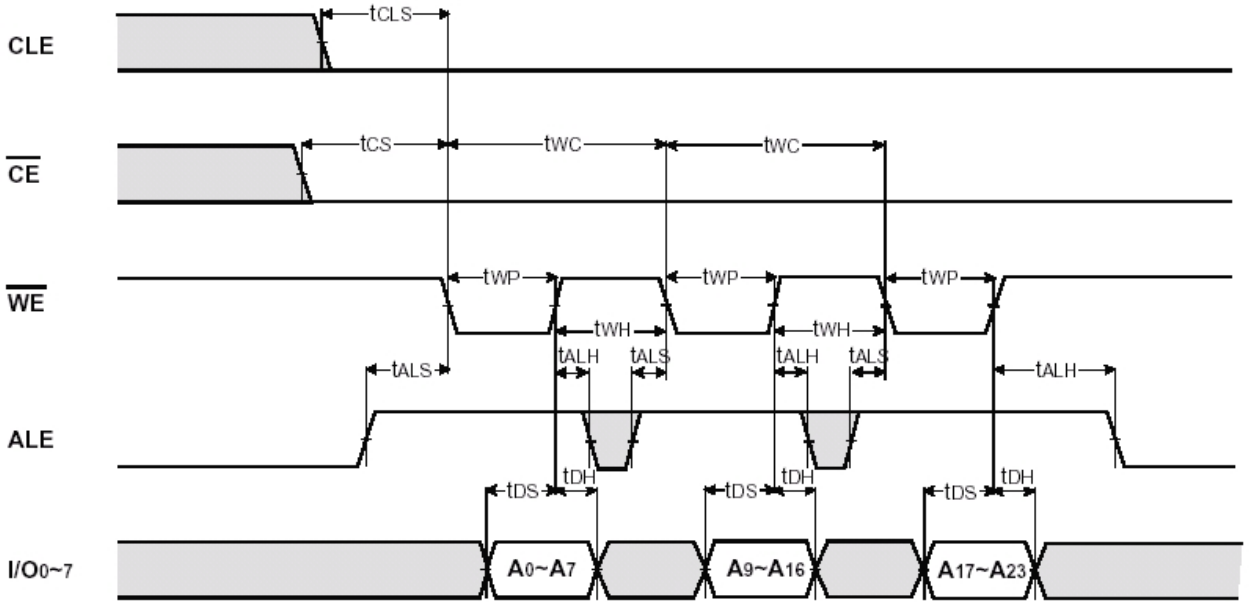
H5.6 Flash Interface Timing

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	53	-	ns
CE Setup Time	t_{CS}	0	-	ns
CE Hold Time	t_{CH}	66	-	ns
WE Pulse Width	t_{WP}	33	-	ns
ALE Setup Time	t_{ALS}	66	-	ns
ALE Hold Time	t_{ALH}	66	-	ns
Data Setup Time	t_{DS}	40	-	ns
Data Hold Time	t_{DH}	25	-	ns
Write Cycle Time	t_{WC}	66	-	ns
WE High Hold Time	t_{WH}	33	-	ns
Read Cycle Time	t_{RC}	66	-	ns
/RE Pulse Width	t_{RP}	44	-	ns
/RE High Hold Time	t_{REH}	22	-	ns
Ready to /RE Low	t_{RR}	66	-	ns

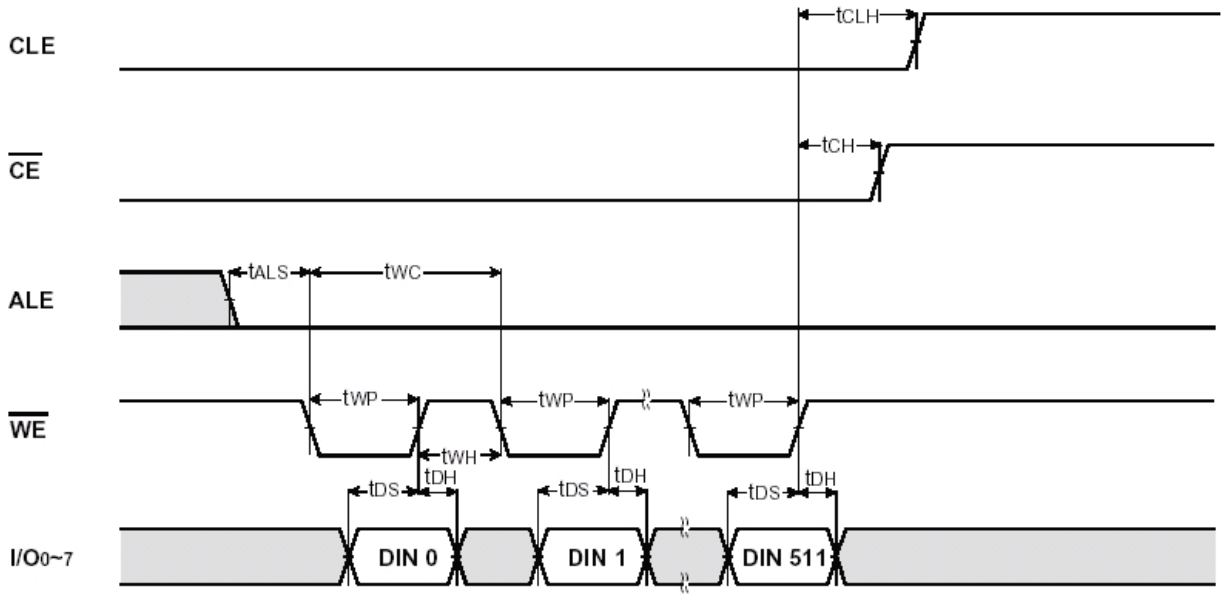
H.5.6.1 Command Latch Cycle



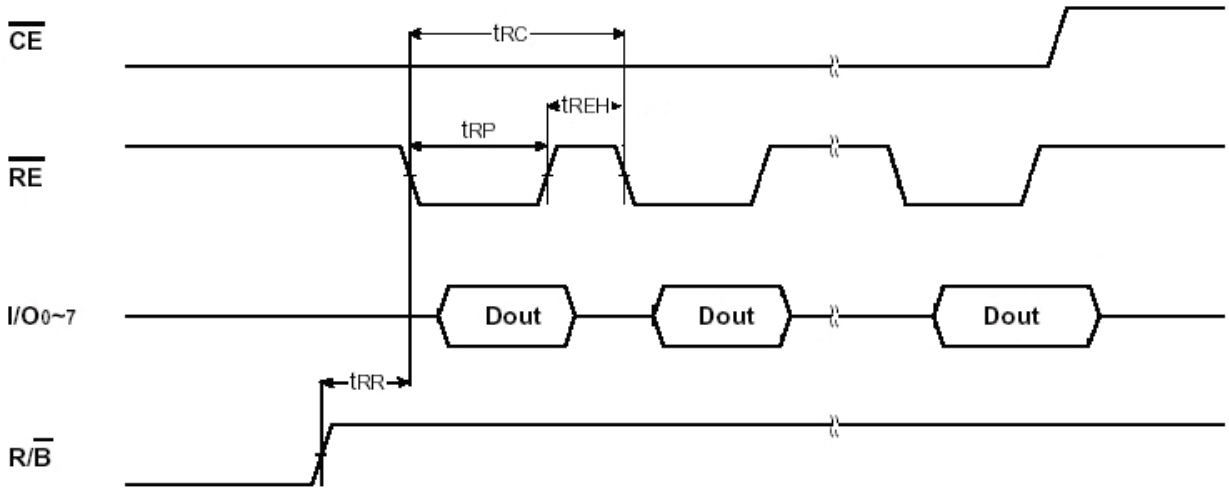
H.5.6.2 Address Latch Cycle



H.5.6.3 Input Data Latch Cycle

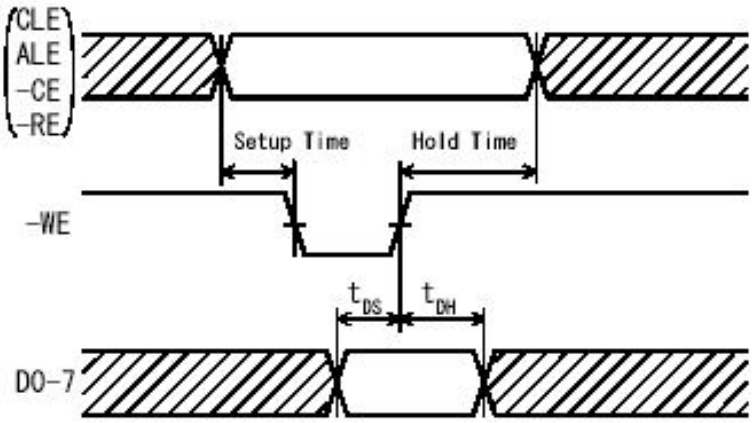


H.5.6.4 Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)

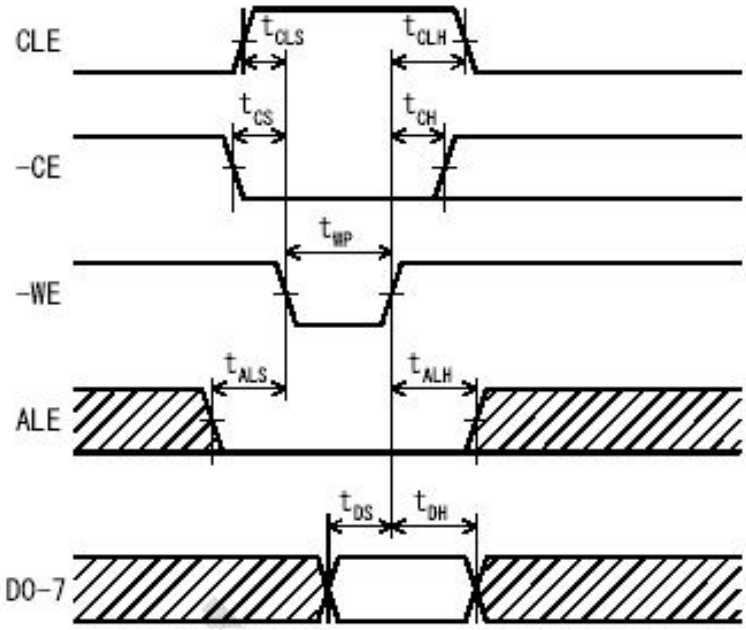


H6. xD-Picture Card Interface Timing

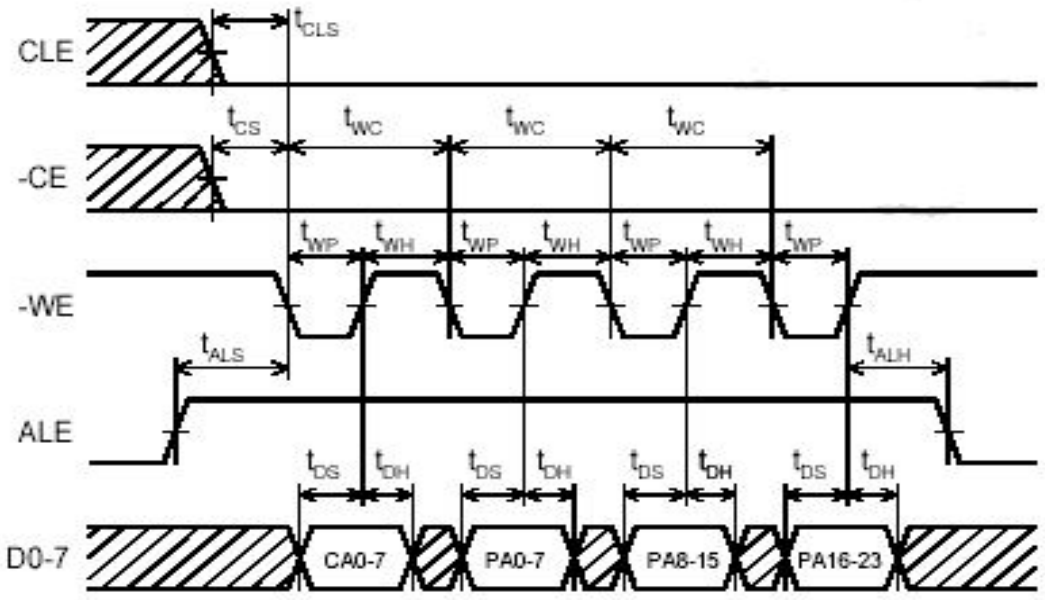
H6.1 Basic latch timing for command and address data



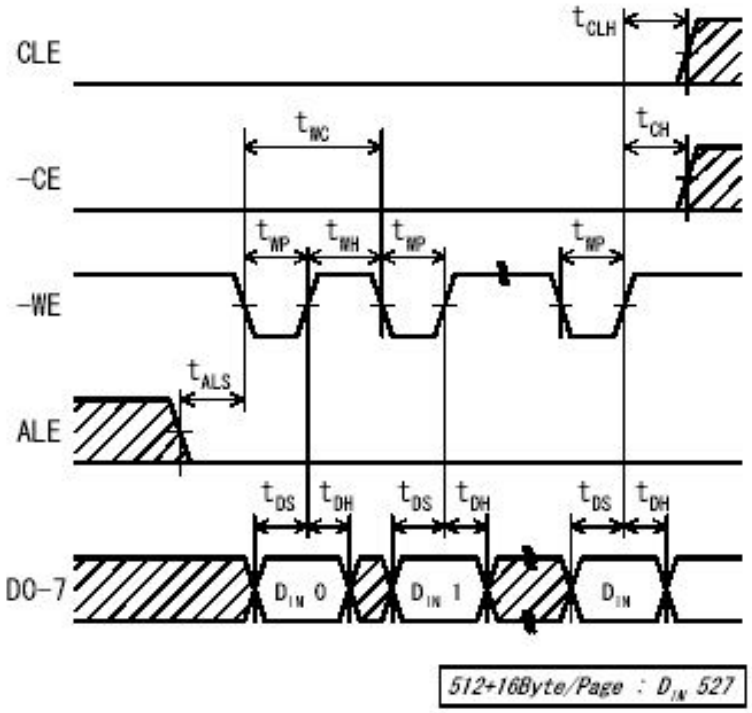
H6.2 Command input cycle



H6.3 Address input cycle

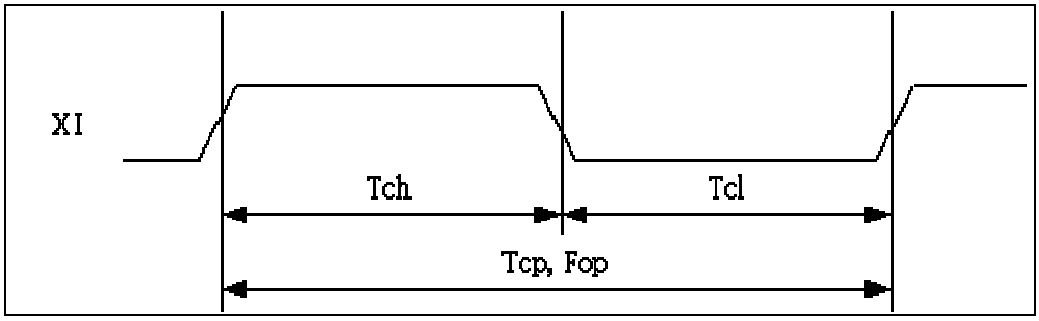


H6.4 Data input cycle



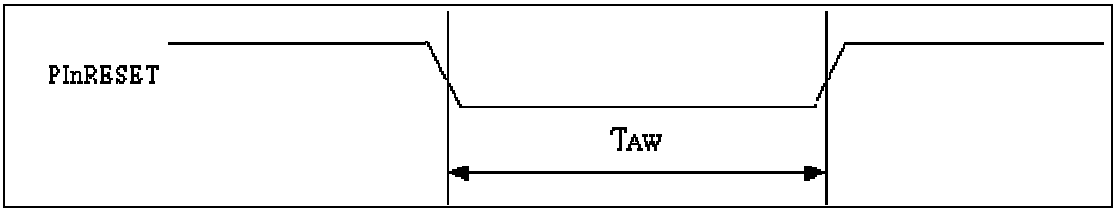
Symbol	Parameter	Min.	Max.	Unit
t_{CLS}	CLE Setup Time	20	-	ns
t_{CLH}	CLE Hold Time	40	-	ns
t_{CS}	-CE Setup Time	20	-	ns
t_{CH}	-CE Hold Time	40	-	ns
t_{WP}	-WE Pulse Width	40	-	ns
t_{ALS}	ALE Setup Time	20	-	ns
t_{ALH}	ALE Hold Time	40	-	ns
t_{DS}	Data Setup Time	30	-	ns
t_{DH}	Data Hold Time	20	-	ns
t_{WC}	Write Cycle Time	80	-	ns
t_{WH}	-WE High Hold Time	20	-	ns
t_{WW}	-WP High to –WE Low	100	-	ns
t_{RR}	Read to –RE Low	20	-	ns
t_{RP}	Read Pulse Width	60	-	ns
t_{RC}	Read Cycle Time	80	-	ns
t_{REA}	-Re Access Time	-	45	ns
t_{CEA}	-CE Access Time	-	55	ns
t_{CEH}	-CE High Hold Time (at the Last Serial Read)	100	-	ns
t_{OH}	Output Data Hold Time	10	-	ns
t_{RHZ}	-RE High to Output Hi-Z	-	30	ns
t_{CHZ}	-CE High to Output Hi-Z	-	20	ns
t_{REH}	-RE High Hold Time	20	-	ns
t_{IR}	Output Hi-Z to –RE Low	0	-	ns
t_{RHW}	-RE High to –WE Low	0	-	ns
t_{WHR}	-WE High to –RE Low	50	-	ns
t_{AR1}	ALE Low to –RE Low (ID Read)	100	-	ns
t_{AR2}	ALE Low to –RE Low (Read Cycle)	50	-	ns
t_{CR}	-CE Low to –RE Low (ID Read)	100	-	ns
t_{WB}	-WE High to Busy	-	200	ns
t_{RB}	Last –RE High to Busy (at Sequential Read)	-	200	ns
t_{CRY}	-CE High to Ready (Note)	-	$6+t_r$ (RY/-BY)	ns

H7. Clock Input Timing



Symbol	Parameter	Min	Max	Unit
Fop	Operating Speed	0	62.5	Mhz
Tcp	Clock Period	16	-	ns
Tch	Clock High	7	-	ns
Tcl	Clock Low	7	-	ns

H8. Reset Input Condition



Symbol	Parameter	Min	Max	Unit
TAW	Reset Width	48	-	ns

Phison Electronics Corporation
2F, RiteKom Building, No.669, Sec 4, Chung Hsing Road, Chutung, Hsinchu, Taiwan 310, R.O.C.
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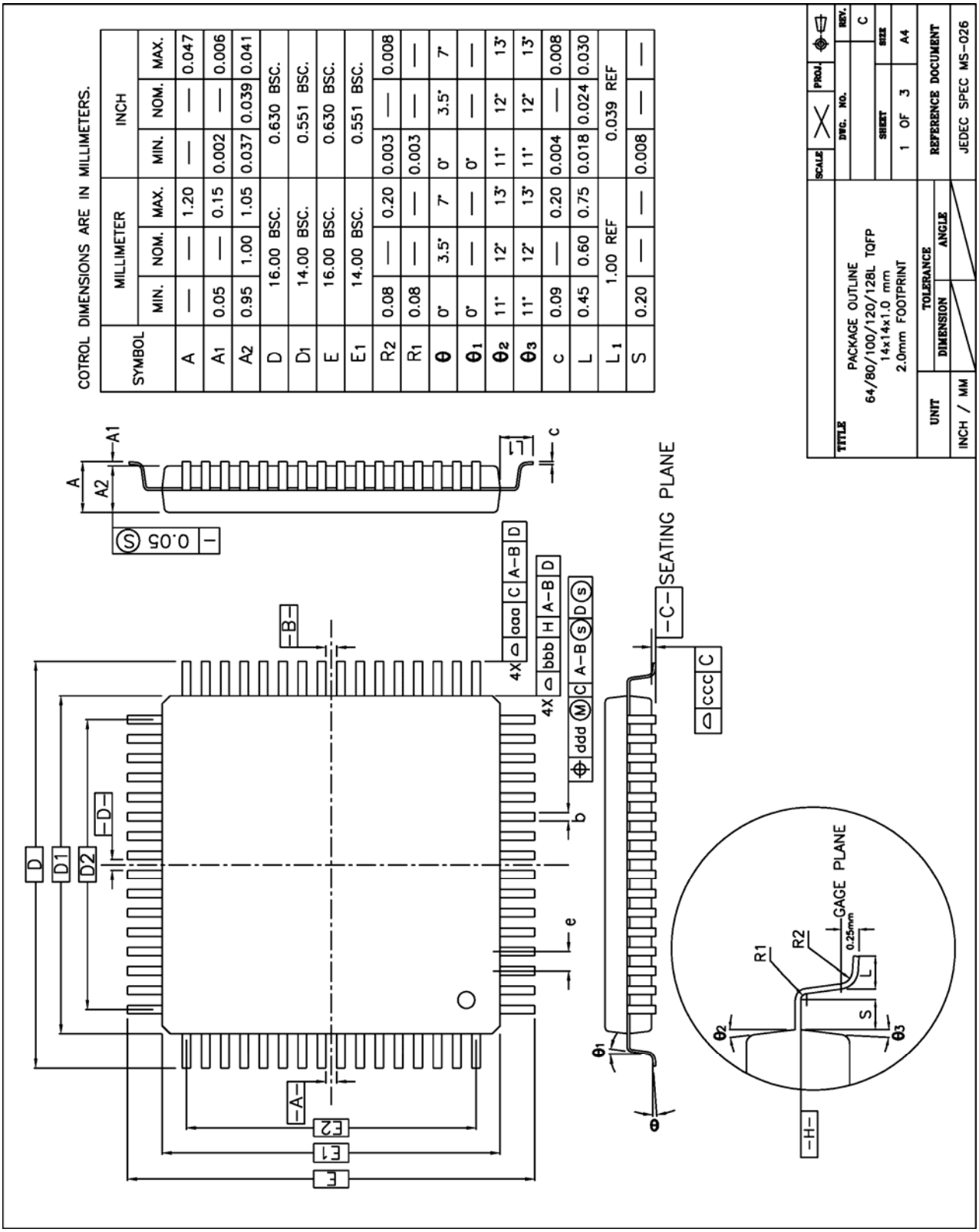
I. Package Specifications

I1. TQFP 128 pins



DCC.: S-06030

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Tel : +886-3-583-3899 Fax : +886-3-583-3666

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

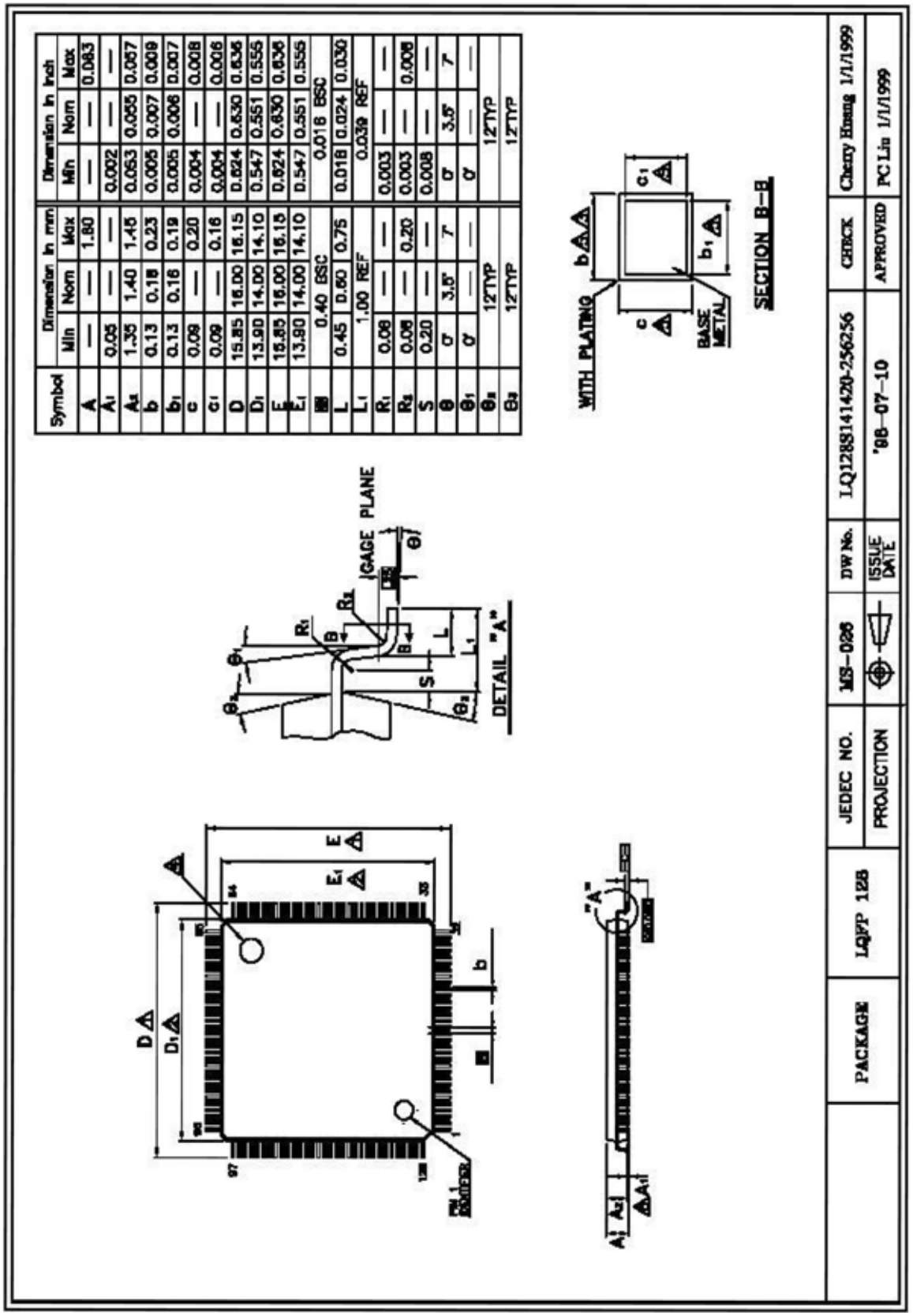
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

			SCALE	PROJ.
TITLE PACKAGE OUTLINE 64/80/100/120/128L TQFP 14x14x1.0 mm 2.0mm FOOTPRINT			DWG. NO.	REV. C
			SHEET 2 OF 3	SIZE A4
UNIT	TOLERANCE DIMENSION	TOLERANCE ANGLE	REFERENCE DOCUMENT	
INCH / MM			JEDEC SPEC MS-026	

2F, RiteKom Building, No.669, Sec 4, Chung Hsing Road, Chutung, Hsinchu, Taiwan 310, R.O.C.
Tel：+886-3-583-3899 Fax：+886-3-583-3666

I2. LQFP 128 pins



DCC.: S-06030